Design and Simulation of a Harmonic Compensator in Power Systems Using Hybrid Parallel Active Filter

A thesis submitted

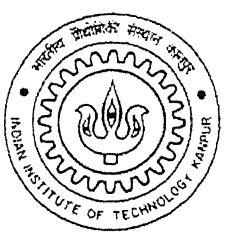
In partial fulfillment of the requirements

for the degree of

Master of Technology

by

Kingshuk Kr. Das



to the

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Certificate

It is certified that the work contained in the thesis entitled, **Design and Simulation of a Harmonic Compensator in Power Systems Using Hybrid Parallel Active Filter**, by Kingshuk Kr. Das, has been carried out under my supervision and this work has not been submitted elsewhere for a degree.

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Abstract

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Proliferation of power electronic loads, a prerequisite for realizing energy efficiency and productivity benefits, has brought utilities to crossroads. Utilities on the one hand are promoting the use of non-linear adjustable speed drive (ASD) loads for significant energy savings to the customer and on the other hand, more frequently encounter harmonic related problems including substantially higher transformer and line losses due to harmonics, required derating of distribution equipment and severe harmonic interactions between customers or between the utility and load, reduced system stability and safe operating margins. Passive filters consisting of capacitors and inductors have long been used to reduce harmonics. Passive filters offer less expensive and simple solution to the harmonics. But passive filters suffer form the danger of resonance at one or more harmonics frequency, which further increases harmonics. Active filters overcome majority of the drawbacks of the passive filters. Pure active filters provide effective solution for a small rating nonlinear load, but are not feasible and cost effective for a large rated non-linear load due to their high rating requirement. Hybrid filters offer a cost effective and practical solution for harmonic filtering and harmonic isolation for large rated nonlinear loads.

In this thesis, a new control aspect for a wide band hybrid parallel active filter is investigated

in detail to solve the harmonic distortion problems on the distribution system with lower cost and higher efficiency. The basic circuit is designed using a parallel resonant *LC* circuit tuned at fundamental frequency and a small-rated active filter composed of high frequency inverter. The band-stop property is intended to prevent flow of fundamental frequency currents into the parallel branch. Low impedance is offered to all harmonic components within the bandwidth of the active filter with proper choice of resonant circuit parameters. This results in a great reduction of the required rating as well as the cost of the active filter.

This work presents the design of control circuit and a hardware scheme for a wide band hybrid active filter. Depending on its bandwidth, the hybrid parallel active filter is capable of compensating multiple harmonic components. This is expected to result in an improved cost effectiveness of the proposed configuration vis-a-vis almost all topologies reported in literature. Special considerations are incorporated to take care of variations in system frequency, noticeable in many utility supplies.

The controller is developed by using *TMS320F240 DSP* processor. A phase lock loop (*PLL*) system is completely implemented in software on this *DSP* and tested in a a 400V/50Hz system. A voltage sensor card is also designed and used in experiment. The step wise procedure for designing of inductor is presented with an example.

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No amount of thanks would be enough for my supervisor, Dr. Partha Sarathi Sensarma. His overly enthusiasm and integral view on research and his idea of providing quality work, has made a deep impression on me. I owe him a lot for having me shown this way of research. Our technical and non-technical discussions kept the spirits high.

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I am extremely grateful to my parents, whose inspiration and encouragement could bring me to the portals of my present achievements in academics. I am also grateful to my sister Pritikana, with whose loving co-operation, I could succeed throughout.

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v Instantaneous value of PCC voltage.

ω Angular frequency of PCC voltage.

θ Phase angle of PCC voltage.

Z_s Line impedance at frequency ω.

L_s Inductance of the Line.

e Instantaneous value of PWM Inverter output voltage.

V_{dc} Nominal value of PWM Inverter dc link voltage.

i PWM Inverter output current.

L_i, R_i Inductance and Resistance of the PWM Inverter ripple filter.

m modulating index for PWM inverter.

Z_f Impedance of the Resonance Filter at frequency ω.

Z Impedance of the Passive Branch at frequency ω.

i_L Load current.

i_{Lh} Load harmonic current.

$*$ Superscript showing reference quantities.

d Subscript showing d-axis component of the quantities transformed to two axes d-q frame.

q Subscript showing q-axis component of the quantities transformed to two axes d-q frame.

dq Subscript showing the quantities transformed to two axes d-q frame.

ref Subscript showing reference quantities.

K_I Integral gain of PI controller.

K_P Proportional gain of PI controller.

u PI controller input.

y PI controller output.

f_{sw} Switching frequency.

Chapter 1

Introduction

Recent development of power semiconductor devices and their application technique has contributed to high efficiency and performance of the industrial apparatus, but simultaneously led to the increase of harmonic interference problems on the electrical distribution system. Harmonic currents drawn from the supply by non-linear loads [1] such as diode or thyristor converters and cycloconverters also result in the distortion of the supply voltage waveform at *PCC* (*"point in the public network which is closest to the consumer concerned and to which other customers are or may be connected" IEC 61000-3-4:1998*) due to the finite supply impedance.

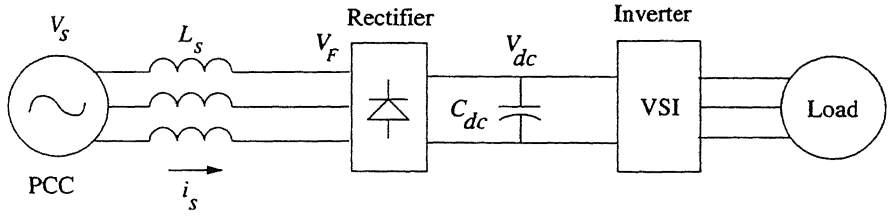

Figure 1.1. Example of a Non-linear load

Many electric utilities are promoting the use of adjustable speed drives (*ASDs*) through aggressive rebate and incentive programs. However, a proliferation of diode and thyristor rectifiers as *ASD* front-ends has resulted in serious utility interface issues as well as power quality degradation such as supply current and voltage harmonics, reactive power, flicker and resonance problems in industrial applications.

Typical types of harmonics :

- Rectifier and thyristor converters feeding the non-linear loads
- Supply side current harmonics: Odd multiple of the fundamental supply frequency (5,7,11,13,....)
- DC side voltage and current harmonics: Even multiple of the fundamental supply frequency
- Arc furnaces can have odd, even multiples as well as sub harmonics
- Non-characteristic harmonics produced due to voltage imbalances or firing angle imbalance in thyristor firings in a converter

Voltage distortion due to current harmonics is becoming a major problem for the utilities at distribution levels. Utilities more frequently encounter harmonic related problems, such as

- Low distortion factor, which results in low power factor
- Harmonic torques in induction motors
  - Torque pulsations
  - Overheating (i.e. Reduction of operating life)
  - Derating (i.e. Under-utilization of motor)
- Speeding-up of electromagnetic energy meters
- Overheating of transformers (due to hysteresis losses)
- Telephonic interference
- Mal-operation of equipment connected to the same bus
- Resonance with supply impedance
- Increased losses in power factor correction capacitors

- Possible interference with power line communication
- Reduced system stability and safe operating margins.

To alleviate harmonic related problems, utilities are beginning to implement harmonic standards such as *IEEE 519* for industrial and large commercial customers, *IEC 61000-3-2, 61000-3-4, 61000-3-12* etc. This increases the need for cost-effective and practical approach to harmonic filtering problem for large non-linear loads to meet *IEEE 519* recommended harmonic standards. It is important to note that *IEEE 519* harmonic standards are only applicable at the point of common coupling (*PCC*) of the utility-plant interface. New specifications often treat it as an equipment standard, a clear misapplication [2].

Passive filters consisting of a bank of tuned LC filters and/or a high-pass filter have been broadly used to suppress harmonics because of a low initial cost and high efficiency. However passive filters have some serious disadvantages due to resonance.

With remarkable progress in the speed and capacity of semiconductors switching devices such as *GTO* thyristors and *IGBT*'s, active filter consisting of voltage or current source *PWM* inverters have been studied and put into practical use because they have the ability to overcome the above mentioned disadvantages inherent in passive filters. But it is difficult to construct a large-rated current source with a rapid current response and the initial costs and running costs are high.

So the use of hybrid active filters has been proposed as a means for combining the lower cost of the passive filters with the control capability offered by a small rating active filter.

Since harmonic compensation by itself does not provide any direct benefit or increased productivity to the user, except through reduced load outages and reduced susceptibility to harmonic related problems, there is seldom any motivation for users to voluntarily meet *IEEE 519* harmonic standards. In fact, harmonic standards often provide a deterrent to the widespread application of ASDs and therefore it does not provide the anticipated energy savings. As a result, some *ASD* manufacturers have started to integrate active filter solutions with *ASD* front-ends to meet *IEEE 519* harmonic standards at the utility-plant interface. To justify the additional cost of harmonic compensation, *ASD* manufacturers provide supplementary value-added features such as

higher displacement power factor (DPF), line voltage regulation against supply voltage sags and swells, compensation for supply voltage flicker and unbalance, and mitigation of any possible source/sink resonance conditions [3].

The organization of the thesis is as follows.

The detail of the harmonic compensation is discussed in second chapter. A few approaches to reduce the rating of the active filters have been proposed on the basis of a combination of active filters and passive elements such as capacitor and reactors. Based on required bandwidth and system cost, a new hybrid active filter topology is proposed, which is capable of compensating multiple harmonic components. This is expected to result in improved cost effectiveness of the proposed configuration vis-a-vis almost all topologies reported in literature.

The design of hardware scheme for a wide band hybrid active filter is discussed in third chapter. The configuration and characteristics for parallel resonant passive elements and switching ripple filter are shown. According to the design procedures the value of the passive circuit components is taken.

A detailed analysis of the filter dynamics is provided in fourth chapter. The state space model is shown for the passive circuit. The Synchronous Reference Frame (*SRF*) controller is implemented for the hybrid parallel active filter. An augmented vector decoupling algorithm is proposed in order to simplify the current control law.

The detail of the simulation is given in fifth chapter. The simulation results for different cases are shown and discussed. Variation of system frequency is incorporated in the simulation. Simulation with mistuned filter is also done.

The sixth chapter is on hardware realization of different sub-modules. *TMS320F240* fixed point *DSP processor* is used to develop the controller. PI controller design for a fixed point processor is derived. Phase transformation module is developed. A low-pass filter is also developed. Details of the *PLL* (phase locked loop) design and the experimental results are included in this chapter. Designing of a voltage sensing card is also shown.

The detail of voltage sensor card designing and manufacturing is given in chapter seven. The designing of a fly-back inductor is also discussed with an example.

Chapter eight is the concluding chapter, summarizes the thesis and points out the direction for possible further work on the hybrid parallel active filter.

Some program modules for using *ADC*, *DAC* and *PWM* channel are included in appendix D. The design of inductor is also shown.

Chapter 2

Harmonic Compensation

In non-linear loads, the current drawn from the utility grid comprises harmonic components in addition to the fundamental, even when the driving voltage consists exclusively of the fundamental component. For distribution systems which must handle a large percentage of non-linear loads, these harmonic currents can be very high. Switch mode power supplies, *PWM* converters, voltage source converters, fluorescent lighting with electronic ballast are some of the major sources of harmonic current.

The additional current will increase losses in wire, bus bars,transformers and power factor correction capacitors used in the distribution system. Harmonic currents flowing through the system impedance result in harmonic voltages at the load. The power factor becomes low due to low distortion factor. Again, due to harmonic currents, the use of line filters before a drive will add more losses to the electrical system and could create line ringing and large voltage transients.

So, to reduce the losses in lines and equipments (copper-loss, core-loss, stray-loss), equipment malfunction and to improve operational efficiency and overall quality of production, harmonic filtering is required.

2.1 Overview of Harmonic Filters

The filters used for harmonic compensation can be broadly classified into two types.

1. **Passive Filter**:

Passive Filters are traditionally series resonant circuits connected in shunt with the non-linear load. In its simplest form, a passive filter circuit is as shown in fig. 2.1. Resonant frequencies of any such passive filter branch is typically tuned to *one* of the dominant harmonics present in the load current.

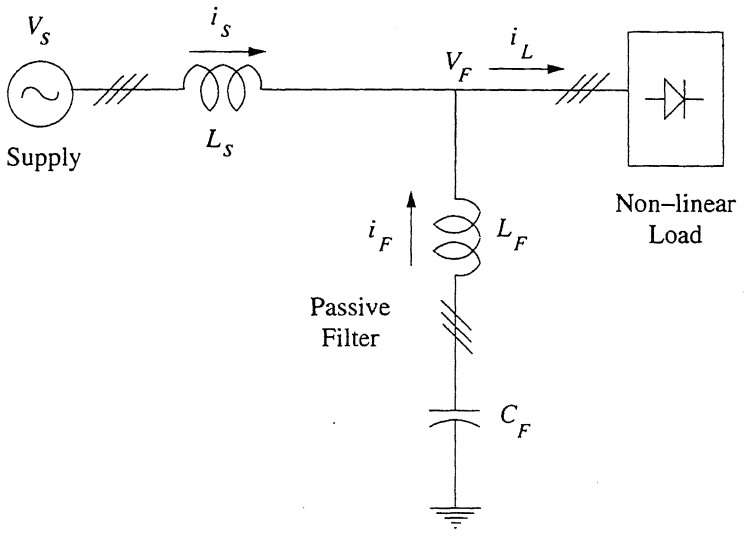

Figure 2.1. Passive Filter

Passive filters have traditionally been used to absorb harmonics generated by large industrial loads, primarily due to their:

- simplicity
- high efficiency
- low cost

Passive filters can also supply reactive power for harmonic generating equipment like 3-phase rectifier load. However, they also have several drawbacks:

- The source impedance strongly influences the filtering characteristics of the passive filter and they are highly susceptible to series and parallel resonance with the source.

  - A passive filter may enter into series resonance with a source so that excessive harmonic current flows into the passive filter.
  - Again the parallel resonance between a source and a passive filter causes amplification of harmonic voltage at *PCC* at specific frequencies.

- Passive filters are sensitive to $L - C$ component tolerances [4, 5, 6]. Tuned passive filters have the problem of attracting harmonic currents from ambient loads and are susceptible to load and line switching transients. Also, due to aging and operating environment, e.g. temperature, the passive components are prone to drift away from their original values of inductance or capacitance. Hence, with time, passive filters almost always are off-tuned with respect to the dominant harmonic frequencies. This defeats their very purpose and intended function as harmonic sinks.
- In particular, for industrial loads connected to stiff supply, it is difficult to design passive filter with sharp tuning and high quality factor, so that it diverts a significant part of the load harmonic current and hence its effectiveness further deteriorates for stiff supply systems [4, 7].

2. **Active Filter**

   Active filters (*AF*) [8, 9] on the other hand comprise intelligent devices which use a voltage source converter to inject a regulated amount of harmonic current of the desired frequency. Various circuit configurations of such active filters are possible but it is more popularly connected in shunt with the non-linear load when used as a current harmonic filter. Schematically, an active filter is connected in circuit as shown in fig. 2.2. Essentially, it behaves as a (voltage controlled) current source, which may be controlled to absorb the harmonic components of the load current.

   Active filters can be classified into the following two types, namely

   (a) pure Active Filter, and

   (b) hybrid Active Filter.

In the subsequent sections of this chapter each of these types are explained along with their special features and characteristics.

2.2 Pure Active Filter

Pure active filter as shown in figure 2.2 has a high frequency voltage-source inverter (VSI) connected to the PCC through coupling inductors. The coupling inductors also serve as ripple filters for filtering the switching frequency components generated by the VSI. Pure Active filters provide effective solution for a small-rating nonlinear load, but are not very cost effective for a large-rating nonlinear load. This is because in a pure active filter, the inverter must generate a fundamental voltage equal and opposite to the *PCC* voltage, so as to block the flow of fundamental current through the AF.

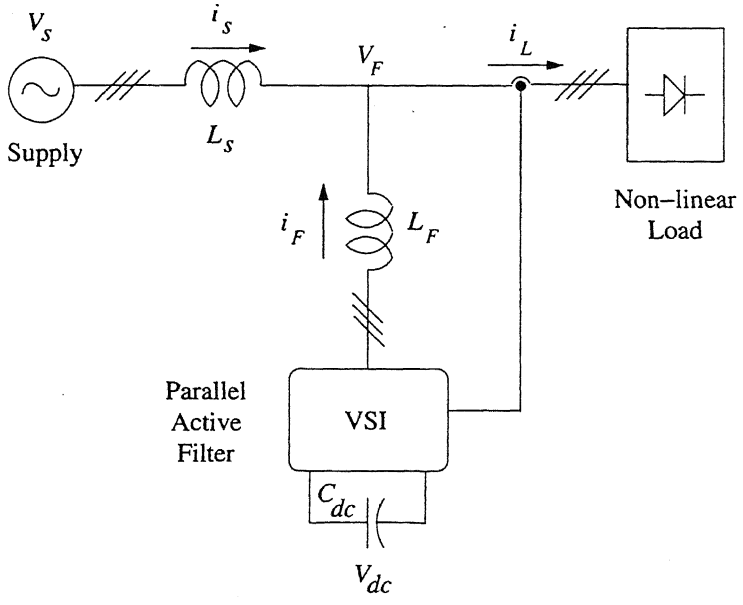

Figure 2.2. Pure Active Filter

Pure active filter systems [8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21] have the following advantages.

- Viable and cost-effective for low to medium kVA industrial loads where system engineering effort is a large part of overall cost.
- Do not create displacement power factor problems and utility loading.
- Network impedances (resonant modes) do not affect the harmonic compensation capability of parallel active filter system.
- Controlled as a harmonic current source.
- Can damp harmonic propagation in a distribution feeder or between two distribution feeders [18].
- Performance is not affected by supply voltage harmonics.
- Protection and sequencing is relatively easy and does not require expensive isolation switchgear.
- Can be installed as a black box solution with minimal system level design expense and provides viable retrofit options.
- Is scalable for higher load kVA rating by paralleling units.

It is to be noted that parallel active filter systems are not suitable for high peak harmonic current loads due to their large rating requirement. Furthermore, for large rated *PWM* inverters with high current bandwidth the dc-bus voltage becomes high for the same current rating, which increase the switching losses. Hence, the efficiency of large rated parallel active filter is a constraint for harmonic compensation at high power levels.

Also parallel active filter systems need to address line interaction of switching ripple filter with supply/load, operation under supply voltage distortion and unbalanced supply/ load conditions [11, 16, 17]. Interactions of the switching ripple filter with supply/ load can be damped within the bandwidth of active filter inverter.

So the use of hybrid active filters has been proposed as a means for combining the lower cost of the passive filters with the control capability offered by a small-rating parallel active filter [10].

2.3 Hybrid Active Filter

Depending on the combination of active filters and passive elements such as capacitors and reactors, hybrid active filters can be broadly classified in the following two categories.

1. **Hybrid Parallel Active Filter**

   The hybrid parallel active filter approach as shown in figure 2.3 is based on the principle of injection of load harmonic currents and hence is characterized by non-sinusoidal current tracking and high current bandwidth requirements [8, 22]. The achieved harmonic compensation characteristics are dependent on the filtering algorithm employed for the extraction of load current harmonics. It has been shown in [7] and [23] that synchronous reference frame-based compensators achieve better performance under all supply and load conditions, and without any assumptions on supply voltage and current waveform quality than state of the art compensators, such as instantaneous reactive power (*IRP*) or p-q theory-based compensators [24] and notch filter-based compensators.

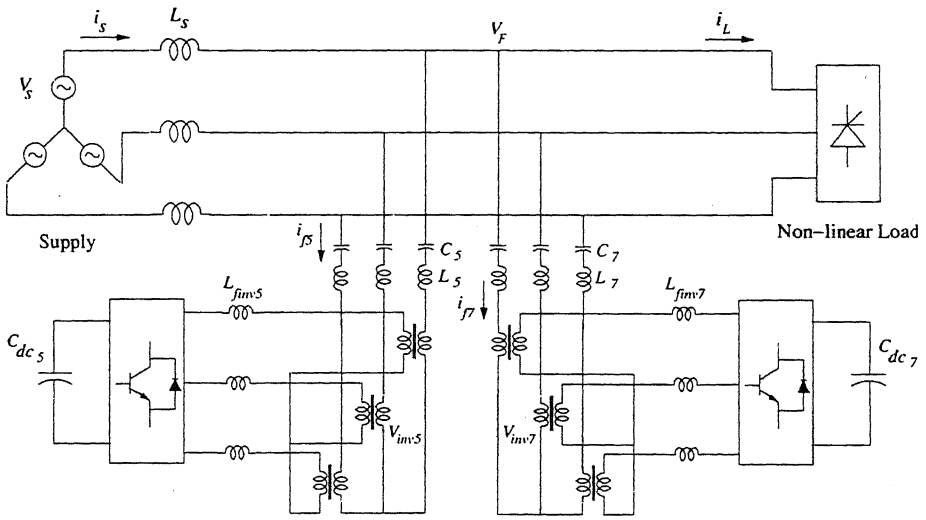

Figure 2.3. Hybrid Parallel Active Filter

2. **Hybrid Series Active Filter**

   The hybrid series active filter consists of a small rated series active filter and tuned L-C pas-

sive filters (may also include high pass filters) as shown in figure 2.4. The active filter has a small rating and is controlled to act as a harmonic isolator between the supply and load by constraining all the load current harmonics to flow into the passive filters. This prevents supply load interaction and eliminates possibility of series and parallel resonances. The harmonic isolation feature reduces the need for precise tuning of passive filters, allow their design to remain relatively unaffected by supply impedance and eliminates possibility of filter overloading due to ambient voltage harmonics and/or ambient harmonic loads. The series active filter allows the passive filters to be exactly tuned to dominant load current harmonics and can also be designed to achieve unity displacement power factor.

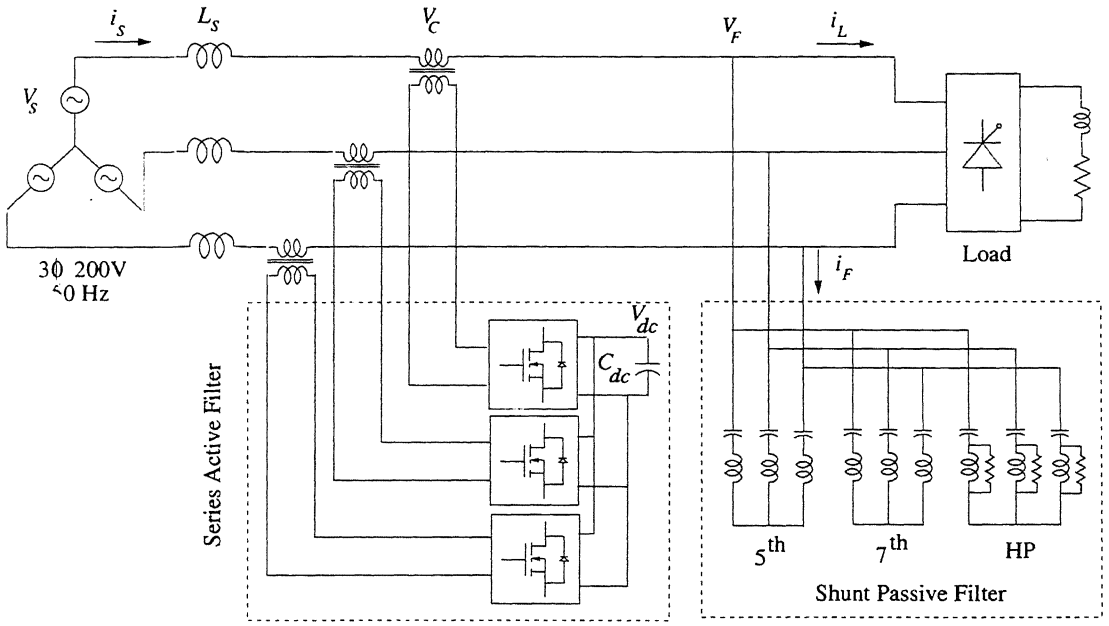

Figure 2.4. Hybrid Series Active Filter

2.3.1 Comparison between Parallel and series Hybrid Active filters

Among the hybrid active filter solutions, parallel hybrid active filters (figure 2.3) offer a practically viable and cost-effective topology for harmonic and reactive power compensation of multiple and diverse high power nonlinear industrial loads, due to small rating of the active filter

$2-3\%$ of load kVA rating and inherent reactive power compensation capability [3, 10, 14].

Further, the hybrid shunt topology is suitable for higher power applications compared to hybrid series topology (figure 2.4), due to easier protection and switchgear requirement.

They also allow retrofit applications with existing LC passive filters or power factor correction capacitors and can provide tuning for off-tuned or mistuned passive filters. They permit passive filter designs to be insensitive to supply line impedances and enable their cost and size optimization.

Hybrid parallel active filter (*HPAF*) systems are particularly suited for harmonic compensation of loads connected to stiff supply systems (low supply impedance). This is because these behave as regulated current sinks rather than frequency-sensitive impedances.

Therefore, the hybrid shunt topology is chosen for the proposed system.

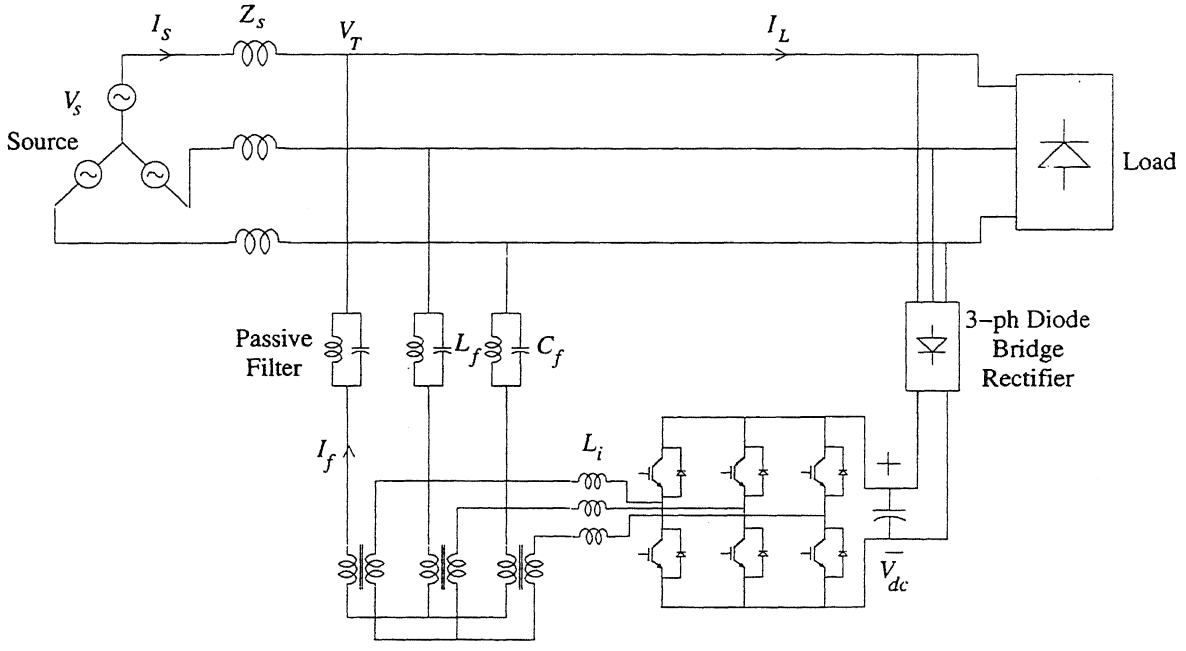

Figure 2.5. Proposed system configuration

2.4 New Topology

A typical single tuned hybrid parallel active filter (*HPAF*) is shown in figure 2.4. But in single tuned hybrid active filter a separate hybrid parallel branch is needed to eliminate each harmonic component as shown in figure 2.4. This greatly adds to the system cost and complexity when multiple harmonic components have to be compensated. This is taken care of in the proposed topology. Depending on its bandwidth, the proposed hybrid active filter is capable of compensating multiple harmonic components. This is expected to result in improved cost effectiveness of the proposed configuration vis-a-vis almost all topologies reported in literature.

Figure 2.5 represents the schematic of the proposed system consisting of an active filter and a passive filter, which are connected in series with each other. The system is installed in parallel with a harmonic producing load, i.e. a 3-phase diode bridge rectifier. The passive filter is a parallel resonant LC circuit tuned at fundamental frequency (50 Hz). It blocks the flow of fundamental current through the filter branch. An inductor (L_i) is connected in series with the VSI output (as a low pass filter) to suppress switching ripples generated by the VSI operation. A 3-phase diode rectifier is used to supply the internal energy losses of the inverter and thus maintain the dc-bus voltage at a constant value.

2.5 Principle of Operation

The parallel branch of the given system shown in figure 2.5 comprises a parallel resonant circuit and active filter. The parallel resonant filter is nominally tuned at the fundamental frequency. The consequent band-stop property is intended to prevent flow of fundamental frequency currents into the parallel branch. With proper choice of resonant circuit parameters, it is possible to ensure that a low impedance is offered to all harmonic components, within the bandwidth of the active filter.

So first of all the load harmonic currents are measured. According to the required harmonic current for a given load, the harmonic voltage is generated in the 3-phase 2-level voltage source *PWM* inverter. Since the parallel resonant circuit blocks the fundamental, the active filter need

not generate any fundamental voltage to cancel out the *PCC* voltage. For this reason the required rating of this inverter is very small. This configuration also ensures that disturbances in the *PCC* voltage magnitude have minimal effect on the filtering performance.

A 3-phase diode rectifier is used in this scheme to supply the dc-bus voltage. The dc-bus voltage is maintained at a constant value through this bridge rectifier. This is connected to the bus in between the load and the parallel branch of the active filter. So the harmonic currents drawn by this bridge rectifier is also supplied through the same active filter. So this parallel branch can be used as a harmonic isolator in between source and load.

2.6 Concluding Remarks

Passive filters consisting of a bank of tuned *LC* filters and/or a high pass filter have been broadly used to suppress harmonics due to their simplicity and low cost, but they have problems with system resonance and off-tuning. Active filters have the ability to overcome the above mentioned disadvantage inherent in passive filters but pure active filter is not appropriate for large-rating nonlinear load due to their high rating requirement. So the use of hybrid active filter has been proposed where the lower cost of the passive filter is combined with the control capability offered by a small-rating parallel active filter. Different type of hybrid active filter topology, proposed in the literature, has been reviewed and their features noted. Among these, hybrid parallel active filter is selected due to their lower rating. A new topology is proposed for a wide band hybrid active filter which is capable of compensating multiple harmonic components. The principle of operation of the proposed circuit is discussed in detail in the subsequent chapters.

Chapter 3

Hardware Design

The hybrid parallel active filter branch of the proposed model is made by series connection of a parallel resonance filter and a switching ripple filter. The passive circuit configuration is shown in figure3.1. The parallel resonance filter consists of one inductor and one capacitor connected in parallel. Basically it is tuned at fundamental frequency to block the flow of fundamental components through this parallel branch. The high frequency PWM inverter generates high frequency switching harmonics, so a switching ripple filter is used in series to eliminate those harmonics. The detail of passive circuit designing is discussed in this chapter.

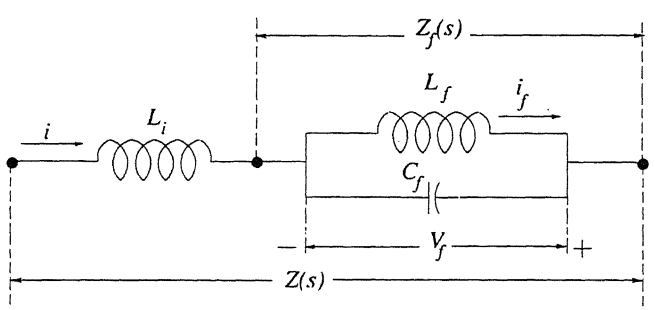

Figure 3.1. Total passive circuit configuration

3.1 Passive Circuit Design

This section details the design of the elements of the passive network. Usual variations of the supply frequency is considered and the design aims to retain adequate filtering properties over the entire range. Also, the effects of mistuning have also been considered.

3.1.1 Parallel Resonance Passive Elements

Configuration

In case of pure active filter as shown in figure2.2, the inverter needs to generate the fundamental voltage according to the *PCC* voltage to stop the flow of fundamental through the parallel branch. So the dc-bus voltage rating increases. As a result the inverter rating as well as the other equipments ratings connected in parallel branch become very high.

So we are interested to use something which can block the flow of fundamental current through the parallel branch and the inverter is not required to generate any fundamental voltage to cancel out the *PCC* voltage.

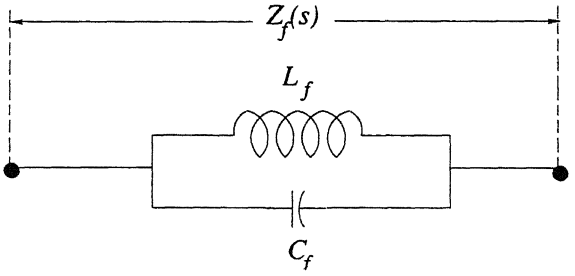

Figure 3.2. Parallel Resonant Circuit

Hence, the parallel resonance filter, as shown in figure3.2, is introduced. The filter is tuned at the fundamental frequency. The consequent band-stop property is intended to block the flow of fundamental current through the parallel branch.

The filter impedance is given by

$$\begin{aligned} Z_f(s) &= (sL_f) \parallel \left(\frac{1}{sC_f}\right) \\ &= \frac{sL_f}{s^2 L_f C_f + 1} . \end{aligned} \tag{3.1}$$

Since the filter is tuned at 50 Hz (fundamental frequency), the admittance of this branch is zero at 50 Hz. Hence for the filter designing

$$s^2 L_f C_f + 1 = 0 ,$$

i.e.

$$\omega_0 = \sqrt{\frac{1}{L_f C_f}} \tag{3.2}$$

where,
ω_0 represents the resonance frequency of the parallel filter.

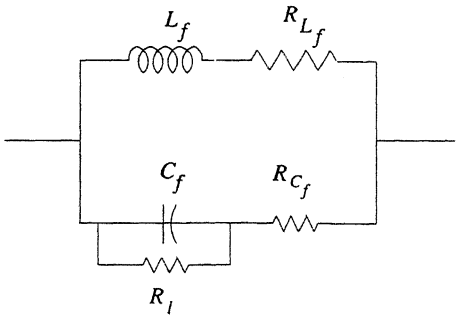

Figure 3.3. Parallel Resonant Circuit

Now 10% resistance is considered for each of the elements of passive circuit.The leakage resistance of capacitor is also considered. So the modified combined impedance of parallel circuit is given by

$$Z_f(s) = \left(sL_f + R_{L_f}\right) \parallel \left(\frac{1}{sC_f} + R_{C_f}\right) \parallel (R_l) \tag{3.3}$$

where,

R_{L_f} and R_{C_f} represent the resistance of L_f and C_f respectively. R_l represents the leakage resistance of the capacitor (C_f) (fig. 3.3).

Characteristics

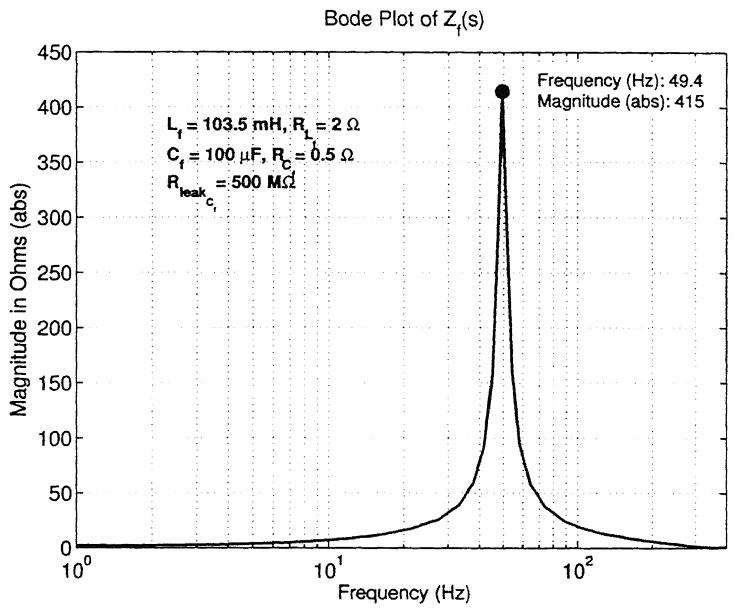

Figure 3.4. Bode magnitude Plot (for $Z_f(s)$)

Figure3.4 represents the Bode plot (magnitude) of parallel resonance circuit. It shows the fundamental component is blocked by the parallel filter, whereas all load harmonic components and the diode rectifier harmonics are passed through this.

In general the impedance of a parallel resonant circuit at cut-off frequency is infinity. But in practical case due to the leakage resistance of capacitor it becomes finite as shown in figure3.4.

Design Consideration

System frequency variation is common in many utility supplies. Generally the frequency variation range is $48 - 51$ Hz. So the passive filter is designed in such a way that it can block the

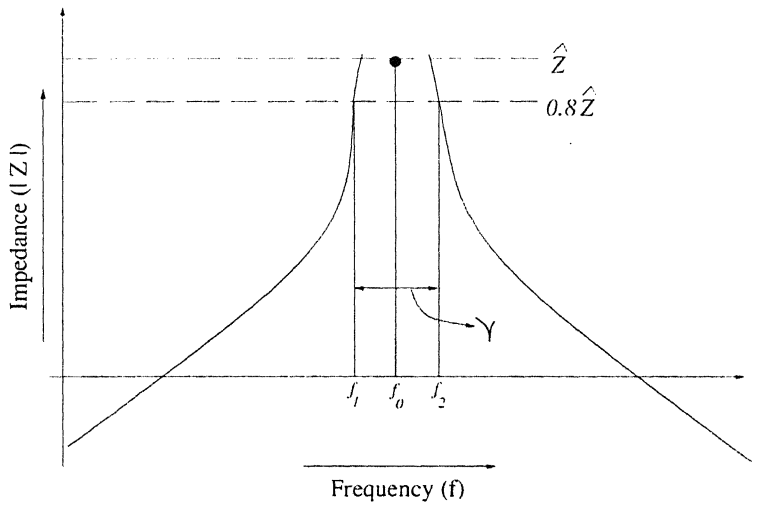

Figure 3.5. Resonant circuit characteristics

fundamental in the range of $48 - 51$ Hz.

In this case the cut-off frequency(f_0) is simply the geometric mean of f_1 and f_2, i.e. cut-off frequency,

$$f_0 = 49.48\ Hz.$$

So if the maximum impedance offered by the filter at cut off frequency (f_0) is taken as $\hat{Z}$, then according to our design consideration at 48 Hz and 51 Hz it must be within $0.8\hat{Z}$ (figure3.5).

As shown in figure3.5, the width of the channel (γ) around cut-off frequency, depends on the chosen value of parallel resonant filter components. A larger γ is required to operate the filter in a frequency variation range. But if γ increases then the impedance offered by this filter for the harmonic components starts rising. So both the cases are taken care of and an optimal solution is chosen.

For low inductance value and large capacitance value, the filter characteristic becomes more selective. Again for small γ and large selectivity (rate of change of impedance with frequency, in between pass-band and stop-band), any change in parameters, change its characteristic.

So the passive filter components L_f and C_f are chosen according to the selectivity of the filter

and the frequency variation range.

Table A.1 contains the values of the parallel resonant filter parameters considered here (in appendix A).

3.1.2 Switching Ripple Filter

A switching ripple filter at the output of the active filter inverter is required to block the high frequency switching harmonic currents produced by the inverter switching.

If effectively designed, switching ripple filters can also provide attenuation for higher harmonic supply currents which are above the current regulator bandwidth of parallel active filter. However, they have the disadvantage of attracting source/sink resonances with supply line inductance L_s, and/or rectifier load.

The inductor L_i, which is connected in series with the inverter, is designed as a low pass filter. The switching frequency of the inverter is 10 kHz. So the value of this inductor is chosen in such a way that it can suppress the switching ripples, which are generated by the inverter.

3.1.3 Total Passive Circuit

The combined impedance of the passive circuit as shown in figure3.1 is given by

$$Z(s) = (sL_i + R_{L_i}) + Z_f(s). \tag{3.4}$$

where,

R_{L_i} is the internal resistance of the switching ripple inductor.

This is the characteristic equation of the passive branch. Bode plot of the total passive circuit impedance, $Z(s)$, is shown in figure 3.6. Figure3.6 represents the Bode plot (magnitude) of the passive branch. It shows the fundamental component and the switching harmonics (greater than 10 kHz) are blocked by the parallel branch, whereas all load harmonic components and the diode rectifier harmonics are passed through it.

Hence only the required load harmonics will pass through this parallel branch, fundamental

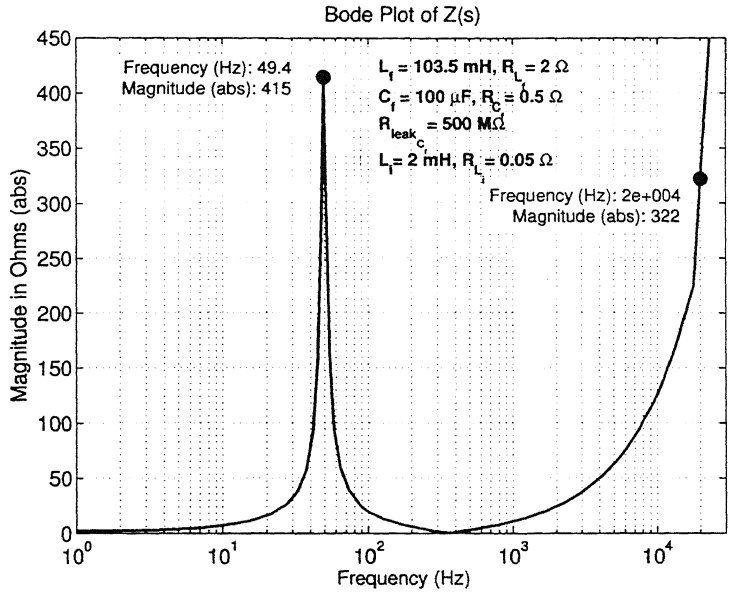

Figure 3.6. Bode magnitude Plot (for $Z(s)$)

and switching harmonics will be blocked. This results in a great reduction of the required rating of the active filter.

3.2 DC bus Capacitance

The voltage and current ratings of passive branch components are decided by the *PCC* voltage and the given load rating. The maximum current flowing through this parallel branch for this given load is 10 amps. The *PCC* voltage is 400 Volts and the frequency is 50 Hz.

The value of the dc-bus capacitor depends on the dc-bus voltage. The dc-bus voltage is taken as 25 Volts for this given system. So according to that the value of the dc-bus capacitor is chosen.

Table A.2 contains the values of the system parameters considered here (in appendix A).

3.3 Concluding Remarks

The passive circuit of the proposed model consists of a parallel resonance filter and a switching ripple filter. According to the principle of operation of the proposed model, the parallel path blocks the flow of fundamental through this branch. So the parallel resonance filter is tuned at fundamental ($50Hz$). Since the passive components are not ideal, 10% resistance is considered for each passive component. The high frequency inverter generates the high frequency switching harmonics, which are not desired. So a switching ripple filter is designed in order to block those switching harmonics. The characteristic of combined passive circuit is analysed. The design considerations are discussed in detail. The frequency variation in the range of $48 - 51$ Hz is also taken into account. The value of the dc-bus capacitor is also selected according to the system parameters.

Chapter 4

Analysis and Control

The detail of dynamic analysis is discussed here. Vector decoupling is introduced to simplify the current control law. A synchronous reference frame (SRF) based current extraction method is used to extract the exact load harmonic currents. The controller is shown in figure4.2. The feedforward control is used to get better dynamic performance.

4.1 Dynamic Analysis

4.1.1 State Space Model Representation

Figure 3.1 is redrawn including the internal resistance for each inductor.

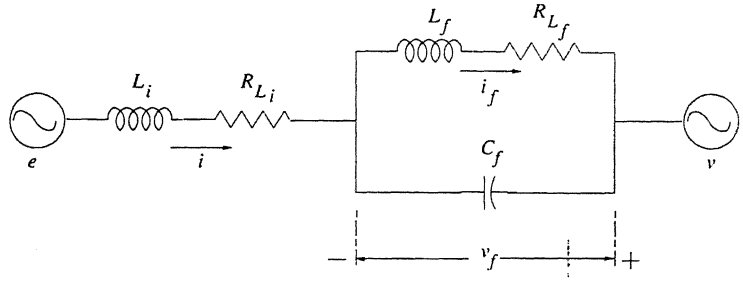

Figure 4.1. Passive Circuit Model

Referring to figure 4.1, the current through L_i, L_f and the voltage across C_f are represented

by i, i_f and v_f respectively and these are used as state variables to represent the state space model of the proposed system.

So the dynamics of the given system is shown by the following equations.

$$i = \frac{1}{L_i}\int (e - v - v_f - iR_{L_i})\,dt$$

$$i_f = \frac{1}{L_f}\int (v_f - i_f R_{L_f})\,dt$$

$$v_f = \frac{1}{C_f}\int (i - i_f)\,dt$$

where,

v is the *PCC* voltage and e is the inverter output voltage.

Now the dynamic equation for three phase system in matrix form is given by

$$\frac{d}{dt}\begin{bmatrix} x_a \\ \cdots \\ x_b \\ \cdots \\ x_c \end{bmatrix} = \begin{bmatrix} A_1 & \vdots & 0 & \vdots & 0 \\ \cdots & \vdots & \cdots & \vdots & \cdots \\ 0 & \vdots & A_1 & \vdots & 0 \\ \cdots & \vdots & \cdots & \vdots & \cdots \\ 0 & \vdots & 0 & \vdots & A_1 \end{bmatrix}\begin{bmatrix} x_a \\ \cdots \\ x_b \\ \cdots \\ x_c \end{bmatrix} + \frac{1}{L_i}\begin{bmatrix} u_a \\ \cdots \\ u_b \\ \cdots \\ u_c \end{bmatrix} \tag{4.1}$$

where,

$$x_a = \begin{bmatrix} i_a \\ i_{fa} \\ v_{fa} \end{bmatrix},\ x_b = \begin{bmatrix} i_b \\ i_{fb} \\ v_{fb} \end{bmatrix},\ x_c = \begin{bmatrix} i_c \\ i_{fc} \\ v_{fc} \end{bmatrix},$$

$$A_1 = \begin{bmatrix} -\frac{R_i}{L_i} & 0 & -\frac{1}{L_i} \\ 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix},$$

$$u_a = \begin{bmatrix} e_a - v_a \\ 0 \\ 0 \end{bmatrix}, \; u_b = \begin{bmatrix} e_b - v_b \\ 0 \\ 0 \end{bmatrix}, \; u_c = \begin{bmatrix} e_c - v_c \\ 0 \\ 0 \end{bmatrix}.$$

Now the 3-phase state space model is transformed into 2-phase state space model by using the following transformation.

$$\begin{bmatrix} x_d^s \\ x_q^s \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}, \tag{4.2}$$

$$\begin{bmatrix} x_d^e \\ x_q^e \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_d^s \\ x_q^s \end{bmatrix}. \tag{4.3}$$

Transformation from 3-phase to 2-phase stationary reference frame is done according to equation(4.2), while equation(4.3) represents the transformation to 2-phase synchronously rotating reference frame.

So the equation(4.1) is modified into the following form.

$$\frac{d}{dt} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} = \begin{bmatrix} A_1 & \vdots & -A_2 \\ \cdots & \vdots & \cdots \\ A_2 & \vdots & A_1 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} + b_c u_c + b_d u_d \tag{4.4}$$

where,

$$x_d = \begin{bmatrix} i_d \\ i_{fd} \\ v_{fd} \end{bmatrix}, \; x_q = \begin{bmatrix} i_q \\ i_{fq} \\ v_{fq} \end{bmatrix},$$

$$A_2 = \begin{bmatrix} \omega & 0 & 0 \\ 0 & \omega & 0 \\ 0 & 0 & \omega \end{bmatrix},$$

$$b_c = b_d = \frac{1}{L_i},$$

$$u_c = \begin{bmatrix} e_d \\ 0 \\ 0 \\ e_q \\ 0 \\ 0 \end{bmatrix}, \; u_d = \begin{bmatrix} -v_d \\ 0 \\ 0 \\ -v_q \\ 0 \\ 0 \end{bmatrix}.$$

Here, u_c is the control input and u_d is the disturbance input.

4.1.2 Vector Decoupling

In equation(4.4), the off-diagonal blocks are nonzero, i.e. the d and q axis quantities are coupled. Basically it represents a multiple-input, multiple-output (*MIMO*) system. The decoupled control of current in *MIMO* system requires a complex current control law. An augmented vector decoupling algorithm [25] is proposed in order to simplify the current control law. Assuming that the system is observable, a first stage of decoupling is achieved as follows.

$$u_c = u_c' + \frac{1}{b_c} \begin{bmatrix} 0 & \vdots & A_2 \\ \cdots & \vdots & \cdots \\ -A_2 & \vdots & 0 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix}.$$

So the equation(4.4) modified into the following form,

$$\frac{d}{dt} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} = \begin{bmatrix} A_1 & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & A_1 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} + b_c u_c' + b_d u_d \,. \tag{4.5}$$

In equation(4.5), the off-diagonal blocks are zero, i.e. the d and q axis quantities are decoupled

but some off-diagonal elements of A_1 are nonzero, which imply the d-axis or q-axis quantities are coupled among themselves. So a second stage of decoupling is achieved as follows.

$$u_c' = u_c'' + \frac{1}{b_c} \begin{bmatrix} A_3 & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & A_3 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix}$$

where,

$$A_3 = \begin{bmatrix} 0 & 0 & \frac{1}{L_i} \\ 0 & 0 & -\frac{1}{L_f} \\ -\frac{1}{C_f} & \frac{1}{C_f} & 0 \end{bmatrix}.$$

Now the system equation modified into the following form.

$$\frac{d}{dt} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} = \begin{bmatrix} A_4 & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & A_4 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} + b_c u_c'' + b_d u_d \tag{4.6}$$

where,

$$A_4 = \begin{bmatrix} -\frac{R_i}{L_i} & 0 & 0 \\ 0 & -\frac{R_f}{L_f} & 0 \\ 0 & 0 & 0 \end{bmatrix}.$$

Thus, to achieve decoupling of states, the following control law is proposed.

$$u_c = u_c'' + \frac{1}{b_c} \begin{bmatrix} A_3 & \vdots & A_2 \\ \cdots & \vdots & \cdots \\ -A_2 & \vdots & A_3 \end{bmatrix} \begin{bmatrix} x_d \\ \cdots \\ x_q \end{bmatrix} \tag{4.7}$$

where,

$$A_2 = \begin{bmatrix} \omega & 0 & 0 \\ 0 & \omega & 0 \\ 0 & 0 & \omega \end{bmatrix},$$

and

$$A_3 = \begin{bmatrix} 0 & 0 & \frac{1}{L_i} \\ 0 & 0 & -\frac{1}{L_f} \\ -\frac{1}{C_f} & \frac{1}{C_f} & 0 \end{bmatrix}.$$

4.2 Control Strategy

The hybrid parallel active filter is controlled to provide its intended function of harmonic isolation between the supply and load by injecting harmonic current according to the load requirement. The parallel branch offers high impedance (ideally, open circuit) at the fundamental frequency and high frequency switching harmonics and low impedance (ideally, zero) at all desired harmonic frequencies. This constrains all load harmonic currents to flow into the passive branch and bypassing the supply. A simple controller implementation is achieved by measurement of the load and filter currents as well as the voltage across the parallel resonant circuit. After extraction of the harmonic components from the load current measurements, the current reference for the VSI is generated. The VSI is controlled as a voltage controlled harmonic current source. The control circuit is shown in figure4.2.

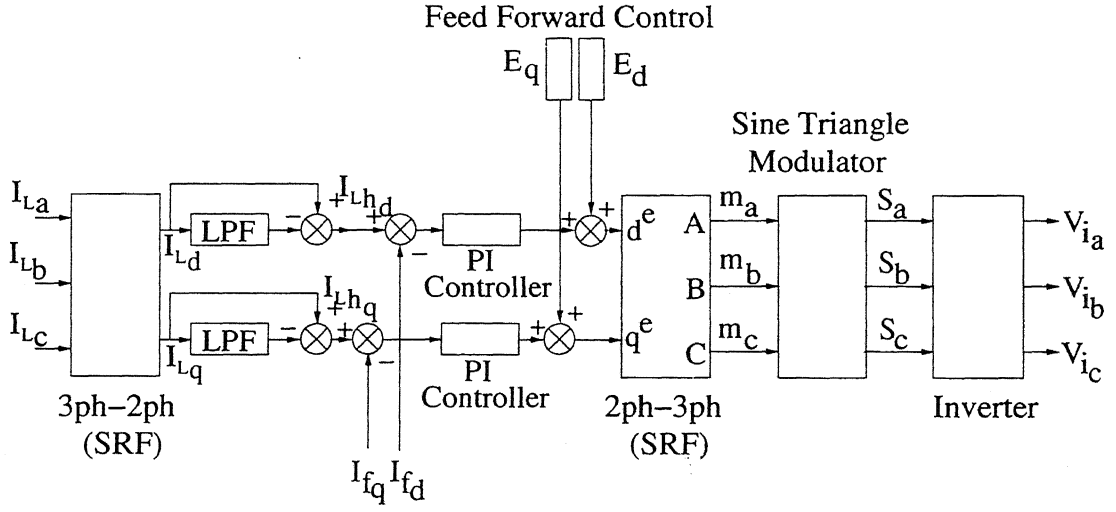

Figure 4.2. Control Scheme

Operation and harmonic isolation feature of the hybrid parallel active filter system is strongly

dependent on the filtering algorithm employed, and the parallel active filter inverter bandwidth. It has been shown that Synchronous Reference Frame (*SRF*) controller achieves significant performance improvement for active filter implementation [7, 22]. Harmonic isolation typically may be required up to the 25^{th} harmonic for commonly used diode rectifier based front-ends for *ASD* loads, which imposes requirement for a significantly higher inverter current bandwidth than inverters employed for motor drive applications.

4.2.1 Synchronous Reference Frame (SRF) Controller

The *SRF* controller proposed by the authors [7, 11, 23, 26] uses the fundamental frequency unit vectors for transformation of the 2-phase currents defined in the stationary reference frame. For any such set of 2-phase currents, $[i^s_{xd} \quad i^s_{xq}]^T$, the following transformation is applied.

$$\begin{bmatrix} {i_{xd}}^e \\ {i_{xq}}^e \end{bmatrix} = [S(\theta_e)] \begin{bmatrix} {i_{xd}}^s \\ {i_{xq}}^s \end{bmatrix}$$

where,

$$[S(\theta_e)] = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix}.$$

The SRF transformation is applied to the inverter and load currents. The transformed signals are used for harmonic extraction as explained below.

In the synchronously rotating $d^e - q^e$ reference frame, the components at the fundamental frequency, are transformed to dc quantities and all the harmonics are transformed to ac quantities and undergo a frequency shift of 50 Hz. So, the extracted signals can be resolved into dc and ac components as follows.

$$\begin{bmatrix} i^s_{xd} \\ i^s_{xq} \end{bmatrix} = \begin{bmatrix} \tilde{i}^s_{xd} \\ \tilde{i}^s_{xq} \end{bmatrix} + \begin{bmatrix} \bar{i}^s_{xd} \\ \bar{i}^s_{xq} \end{bmatrix}. \tag{4.8}$$

The first vector on the right comprises ac quantities and the second comprises dc quantities.

Information about the harmonic components is contained in the first term which is therefore the term of interest.

SRF controller extracts the dc quantities by a low-pass filter (*LPF*). The LPF outputs are then subtracted from the original transform output to obtain the required ac quantities (as shown in fig. 4.2). As the LPF extracts the dc component, it is insensitive to phase errors. This is a significant advantage of the SRF controller since most other controllers will introduce significant phase errors at fundamental and at harmonic frequencies [13, 27, 28].

The SRF controller is implemented by digital hardware. A *DSP* based implementation is made for ease of debugging in the field installation.

4.2.2 Feedback Control

Figure 4.2 shows the feedback controller of the hybrid parallel active filter system. The feedback controller employs *PI* regulators to drive the harmonic components of load currents, and to zero to achieve harmonic isolation.

The harmonic part of the inverter output currents are compared with the load current reference values. The current error is fed into a *PI* regulator which generates the feedback voltage command. Feedforward voltage command, and feedback voltage command , are added to form the harmonic voltage reference for the VSI.

An inverse *SRF* transformation at the same rotation frequency (as the previous forward transformation) is applied and generate corresponding three-phase inverter voltage commands which are then used to generate inverter gate signals.

4.2.3 Feedforward Control

From equation(4.7) the feed-forward component is obtained. So to control the inverter current, $(v_{f_d} + \omega L_i i_q)$ is injected for d-axis feed forward control and $(v_{f_q} - \omega L_i i_d)$ for q-axis feed forward

control, i.e.

$$E_d = (v_{fd} + \omega L_i i_q), \tag{4.9}$$

$$E_q = (v_{fq} - \omega L_i i_d). \tag{4.10}$$

The linear control law can be written in the following form.

$$y_d[k] = K_P u_d[k] + I_d[k] + K_I\{u_d[k] + u_d[k-1]\} + (v_{fd} + \omega L_i i_q)\frac{2}{V_{dc}},$$

$$y_q[k] = K_P u_q[k] + I_q[k] + K_I\{u_q[k] + u_q[k-1]\} + (v_{fq} + \omega L_i i_d)\frac{2}{V_{dc}}.$$

where,

$I[k]$ is initial conditions of the integrator, during k^{th} switching interval. The ripple in the dc bus voltage will be reflected in ac side. So before adding the feed forward part with the error, $\frac{2}{V_{dc}}$ is multiplied with E_d and E_q.

So the dynamic equation of inverter current is modified as follows.

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -\frac{R_i}{L_i} & 0 \\ 0 & -\frac{R_i}{L_i} \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_i}\begin{bmatrix} e_d - v_d \\ e_q - v_q \end{bmatrix}. \tag{4.11}$$

Feedforward command improves the dynamic performance of the hybrid parallel filter system.

In equation(4.11), the *PCC* voltages act as disturbance input to the system, which introduce error into the system performance. This error needs to be kept within acceptable limits and for this reason also feed-forward compensation is required. Since the parallel resonant circuit blocks the fundamental, no need to add *PCC* voltages (v_d and v_q) in feed-forward control. This is the main reason for which the rating of inverter reduces significantly.

4.2.4 Linear Controller

A *PI* controller is used to reduce the steady state error. The control law in discrete-time domain is given by

$$y[k] = K_P u[k] + I[k] + K_I\{u[k] + u[k-1]\} \tag{4.12}$$

where,

$I[k]$ is initial conditions of the integrator, during k^{th} switching interval. The controller parameters are obtained as follows.

Transfer function of the plant is

$$G(s) = \frac{\frac{V_{dc}}{2}}{R + sL} = \frac{\frac{V_{dc}}{2R}}{1 + \left(\frac{L}{R}\right)s}. \tag{4.13}$$

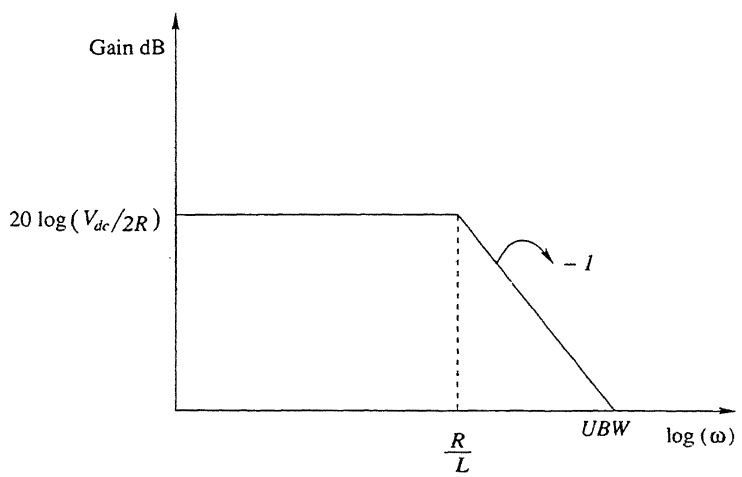

Figure 4.3. Bode plot of Loop Transfer Function With Unity Gain Controller

Let the transfer function of controller be $C(s)$. Approximate Bode plot of loop transfer function with unity gain controller is shown in figure4.3. From figure4.3 it is clear that bandwidth of the system with unity gain controller is

$$UBW = \frac{V_{dc}}{2L} \; rad/sec.$$

The transfer function of the PI controller is

$$C(s) = \left(K_P + \frac{K_I}{s}\right) = K\left(\frac{1+\frac{s}{w_c}}{\frac{s}{w_c}}\right) \tag{4.14}$$

where,

$$K = K_P \tag{4.15}$$

$$w_c = K_I/K_P\ . \tag{4.16}$$

If the closed-loop bandwidth of the system is CBW and settling time is T_{stl}, then,

$$CBW = \frac{4}{T_{stl}}\ . \tag{4.17}$$

The values of K_P and K_I, which result in specified settling time are obtained by considering the following two cases.

1. When $UBW < CBW$

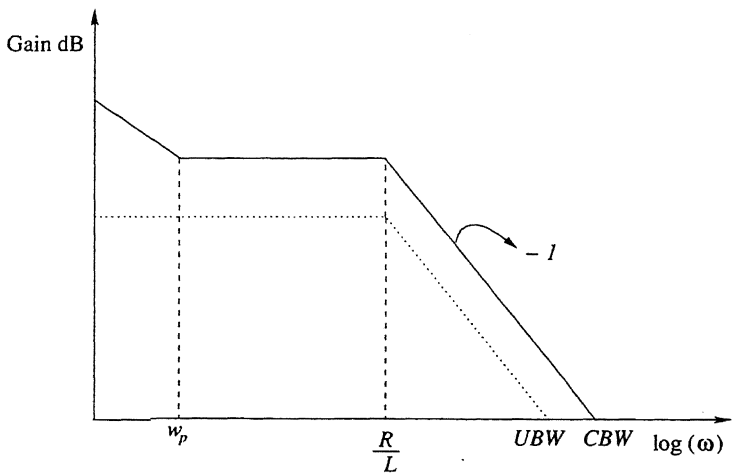

Figure 4.4. Bode plot of Loop Transfer Function When $UBW < CBW$

Bode plot of the loop transfer function $G(s)C(s)$ for this case is shown in figure4.4. It is

obvious that

$$K = \frac{CBW}{UBW} . \tag{4.18}$$

The corner frequency of the controller is selected one decade before the UBW, i.e. $w_c = \frac{UBW}{10}$ rad/sec. So, from (4.15) and (4.16), K_P, K_I can be calculated.

2. When $UBW > CBW$

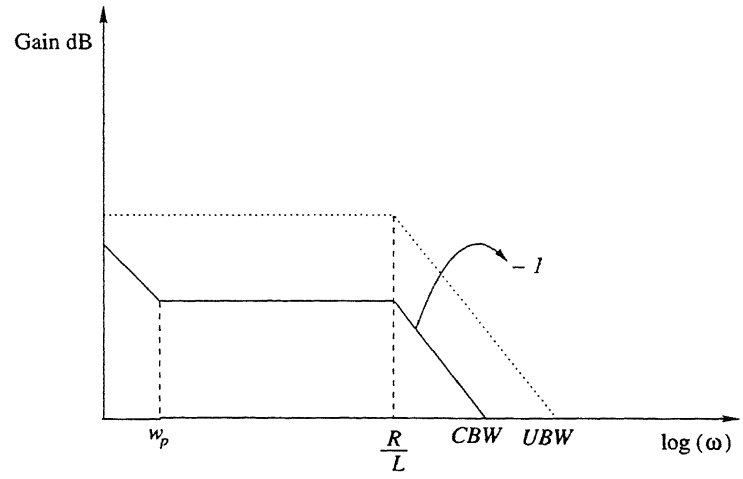

Figure 4.5. Bode plot of Loop Transfer Function When $UBW > CBW$

Bode plot of loop transfer function $G(s)C(s)$ for this case is shown in figure.4.5. The value of K is obtained from equation(4.18), same as before.

The corner frequency of the controller is selected one decade before the corner frequency of the plant $\frac{R}{L}$ rad/sec, i.e. $w_c = \frac{R}{10L}$ rad/sec. So, from (4.15) and (4.16), K_P, K_I can be calculated.

4.3 Concluding Remarks

The dynamic equation of the proposed system is derived. Vector decoupling method is used to simplify the current control law. The control strategy is discussed in detail. The synchronous reference frame (*SRF*) based current extraction method is used to extract the harmonic components from load current and inverter current. A *PI* controller is taken to reduce the steady state error. Feedforward control is added to achieve better dynamic performance.

Chapter 5

Simulation Results and Discussion

The simulation model of the hybrid parallel active filter system is shown in figure 5.1. Parallel resonance filter ($L_f \| C_f$) is connected in series with inverter output. It blocks the flow of fundamental component through the parallel hybrid active filter branch. So it is tuned at fundamental frequency. A switching ripple filter is also connected at the output of inverter and in series with parallel resonance filter. This is used to prevent the switching harmonics. A 3-phase diode bridge rectifier is used as a non-linear load. It is capable to distort the supply current waveforms. So due to finite line impedance the *PCC* voltage also become distorted.

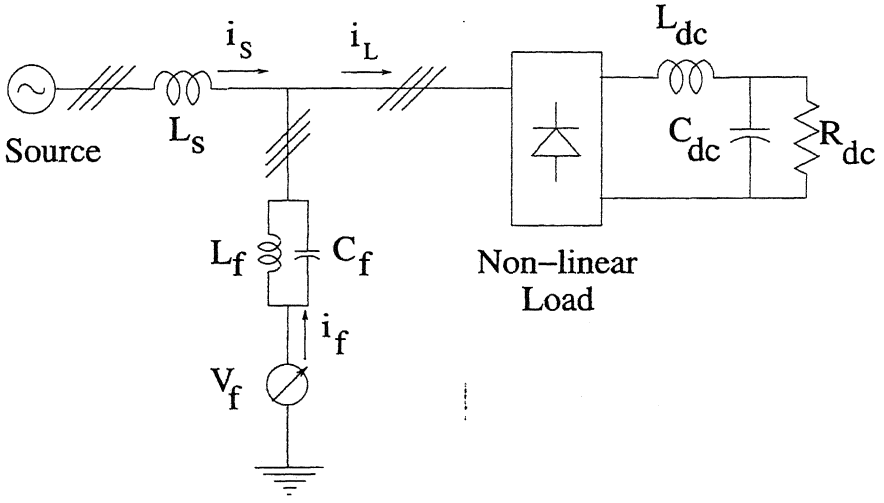

Figure 5.1. Simulation Model

MATLAB simulink is used to develop the simulation model. *MATLAB* is a dynamic technical language and development environment for analyzing data and developing algorithms and applications. *Matlab simulink* is a platform for multidomain simulation and Model-Based Design for dynamic systems. It provides an interactive graphical environment and a customizable set of block libraries, and can be extended for specialized applications.

The basic math blocks are used to make the inductor, capacitor, rectifier, inverter. The leakage resistance of capacitor is not considered.

5.1 Simulation Parameters

The system parameters are listed as below:

Supply voltage, $V_s = 400V$ (line to line rms), i.e. $V_ph = 230V$,

Supply frequency, $f = 50Hz$.

The load is a diode bridge rectifier, 16 kVA, 20 Amps (rms).

Passive filter components usually have tolerances of $\pm 10\%$. The inductor L_f in mistuned passive filter is considered as $0.9L_f$ and the capacitor C_f is taken as $1.1C_f$.

The circuit parameters for parallel resonance filter, switching ripple filter and others, which are used in simulation are shown in appendix B.

Here the system short circuit ratio (*SCR*) is 8, for which $IEEE$ 519 line current total harmonic distortion limit is 5% with 4% limits on 5^{th} and 7^{th} harmoniics, 2% limits on 11^{th} and 13^{th} harmoniics, 1.5% limits on 17^{th} and 19^{th} harmoniics and 0.6% limits on 23^{th} and 25^{th} harmoniics.

5.2 Simulation Results

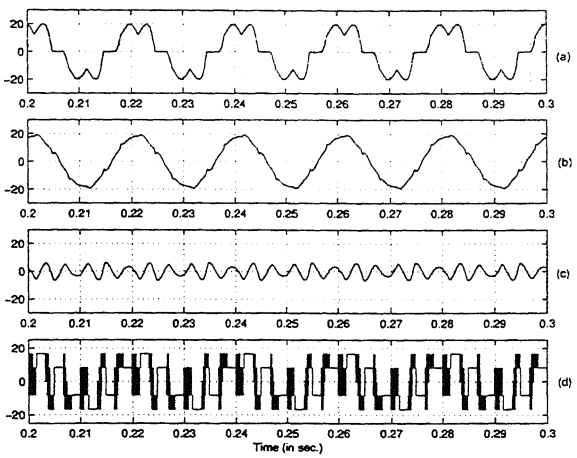

Figure 5.2. Simulation Waveforms (with minimum dc bus voltage 25V): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

Fig. 5.2 shows the simulation results with 25V dc bus voltage. Here the source harmonic currents remain within *IEEE 519* recommended harmonic standards. It is the minimum required dc bus voltage to supply the load harmonic currents.

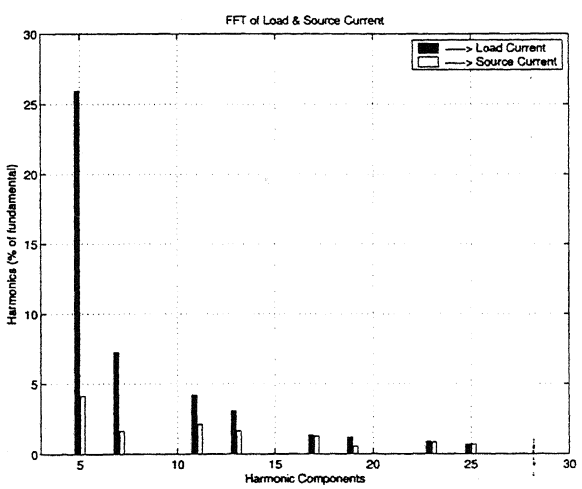

Figure 5.3. FFT of currents for the above case

The harmonic analysis for the load current and the source current is shown in fig. 5.3. The

Fast Fourier Transform (FFT) is used for harmonic analysis. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 4%, 1.65%, 2% and 1.6% respectively, which are less than the standard values. Fig. 5.4 shows the simulation results with 90V dc bus voltage. It is the maximum

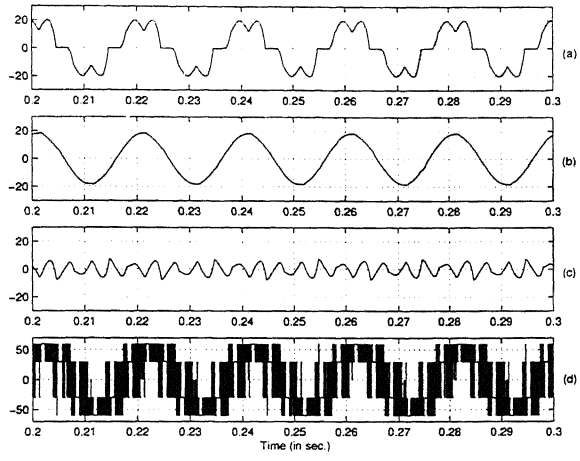

Figure 5.4. Simulation Waveforms (with maximum dc bus voltage 90V): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

required dc bus voltage to supply the all load harmonic currents and to make the supply totally harmonic free.

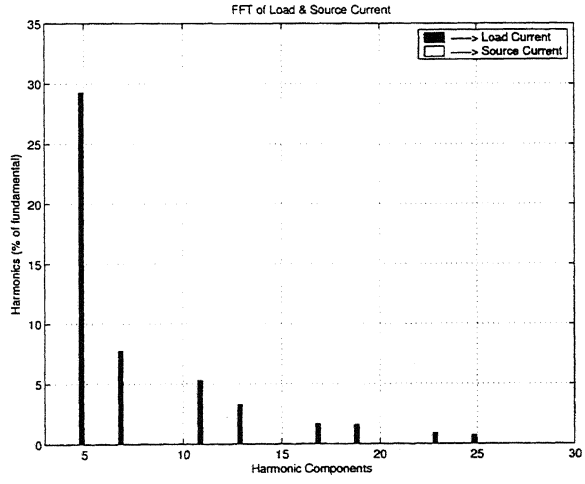

Figure 5.5. FFT of currents for the above case

The harmonic analysis for the load current and the source current is shown in fig. 5.5. It shows the hybrid parallel active filter works as a harmonic isolator in between load and source, i.e. the total load harmonic currents is supplied by active filter.

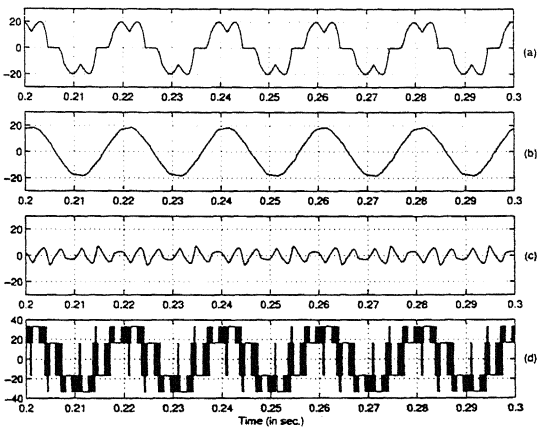

Figure 5.6. Simulation Waveforms at 50 Hz (with tuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

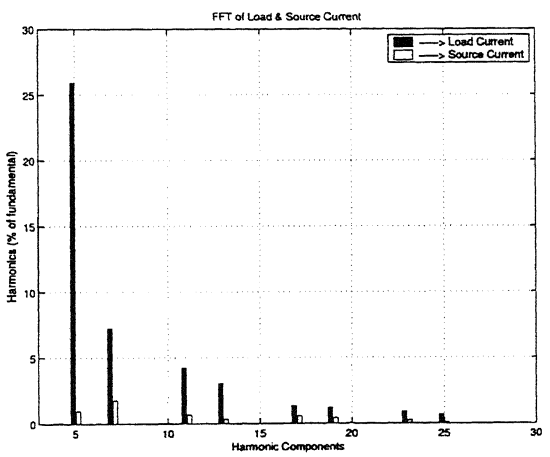

Figure 5.7. FFT of currents for the above case

Fig. 5.6 shows the simulation results at 50Hz supply frequency with tuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.7. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 0.84%, 1.67%, 0.5% and 0.55% respectively, which are much less than the standard values.

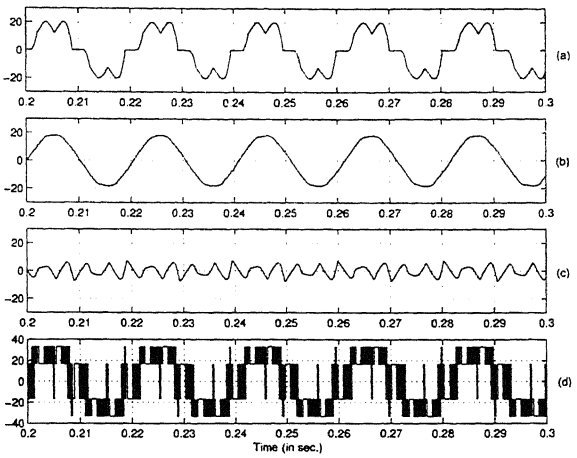

Figure 5.8. Simulation Waveforms at 49 Hz (with tuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

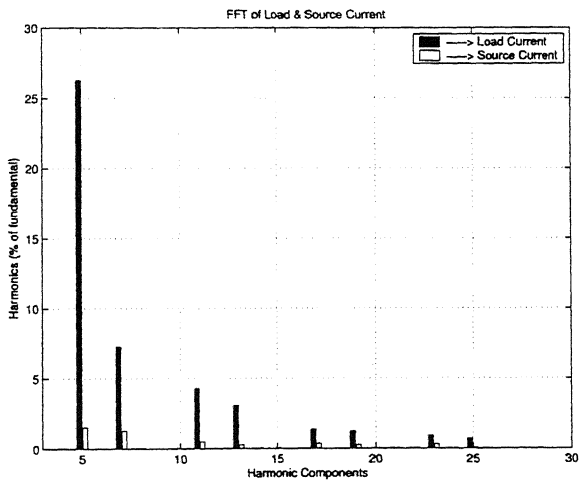

Figure 5.9. FFT of currents for the above case

Fig. 5.8 shows the simulation results at 49Hz supply frequency with tuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.9. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.22%, 1.18%, 0.5% and 0.26% respectively, which are less than the standard values. So the frequency variation does not effect the filter characteristic significantly.

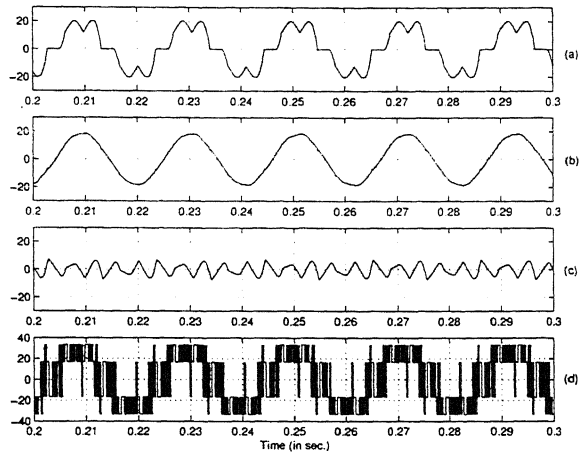

Figure 5.10. Simulation Waveforms at 48 Hz (with tuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

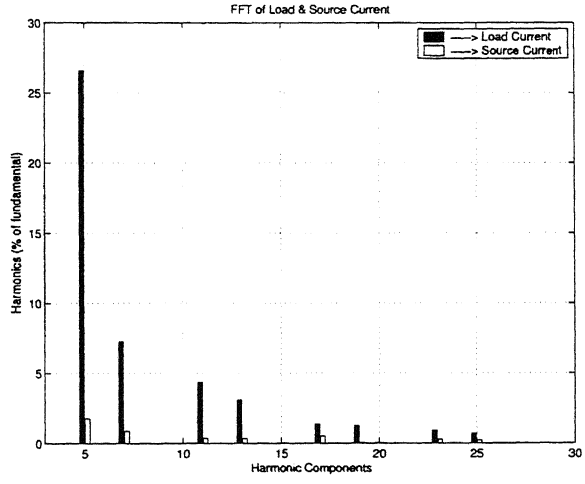

Figure 5.11. FFT of currents for the above case

Fig. 5.10 shows the simulation results at 48Hz supply frequency with tuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.11. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.54%, 0.73%, 0.32% and 0.34% respectively, which are less than the standard values. It implies, this much of frequency variation in negative side can take care of by this HPAF.

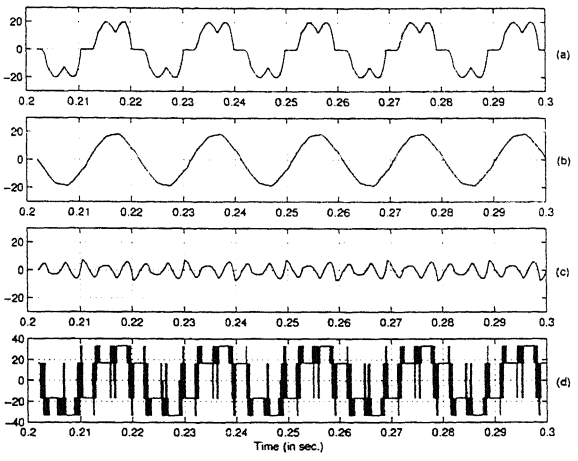

Figure 5.12. Simulation Waveforms at 51 Hz (with tuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

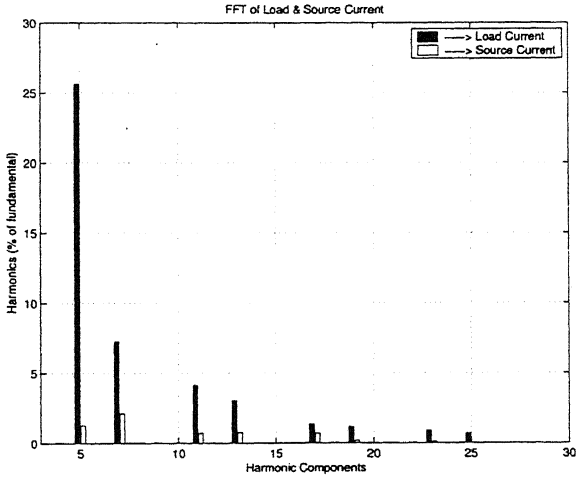

Figure 5.13. FFT of currents for the above case

Fig. 5.12 shows the simulation results at 51Hz supply frequency with tuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.13. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.57%, 1.9%, 0.8% and 0.87% respectively, which are less than the standard values. It implies this much of frequency variation in positive side can take care of by this HPAF.

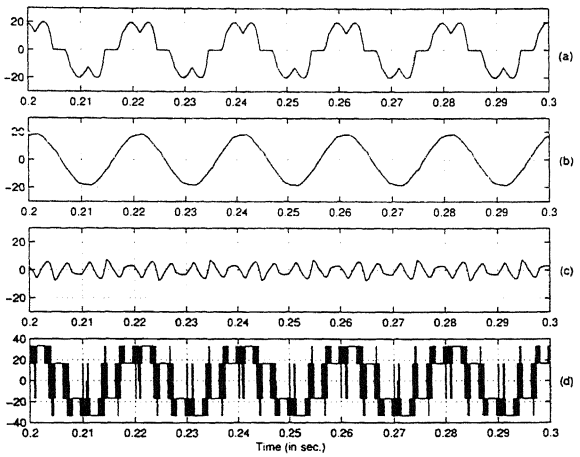

Figure 5.14. Simulation Waveforms at 50 Hz (with mistuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

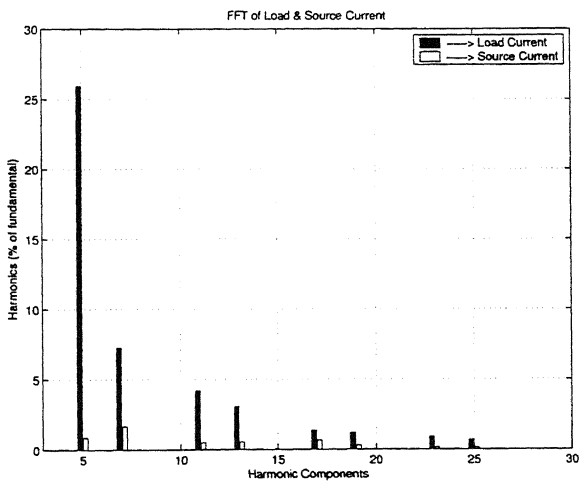

Figure 5.15. FFT of currents for the above case

Fig. 5.14 shows the simulation results at 50Hz supply frequency with mistuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.15. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 0.95%, 1.75%, 0.68% and 0.32% respectively, which are much less than the standard values. So the mistuning does not effect the filter characteristic significantly.

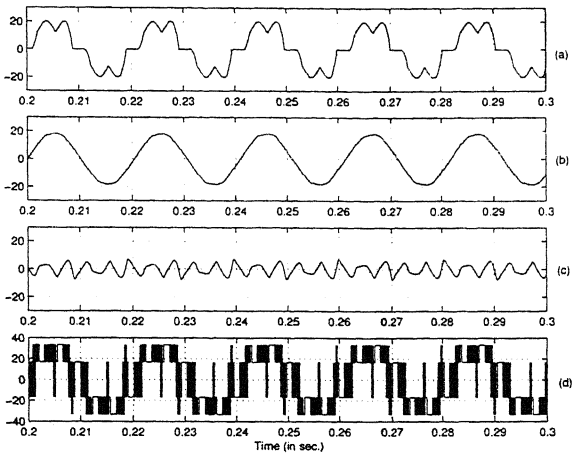

Figure 5.16. Simulation Waveforms at 49 Hz (with mistuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

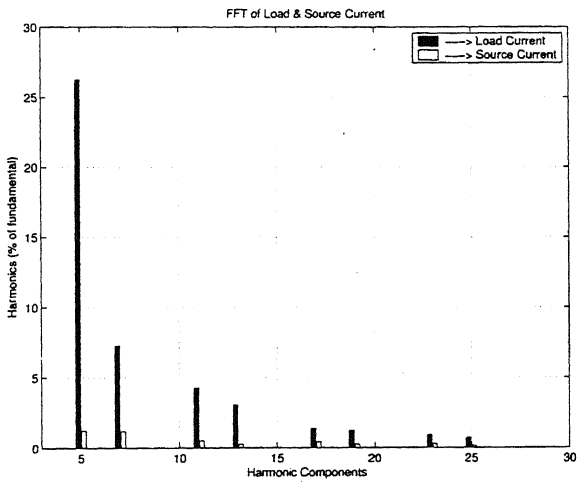

Figure 5.17. FFT of currents for the above case

Fig. 5.16 shows the simulation results at 49Hz supply frequency with mistuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.17. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.5%, 1.25%, 0.5% and 0.27% respectively, which are less than the standard values. So the frequency variation does not effect the filter characteristic significantly in case of a mistuned passive filter.

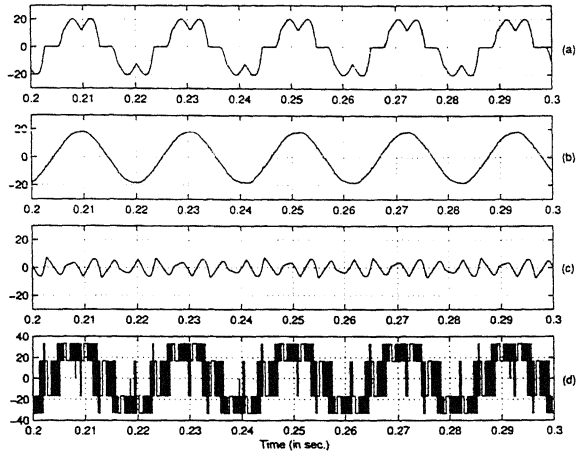

Figure 5.18. Simulation Waveforms at 48 Hz (with mistuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

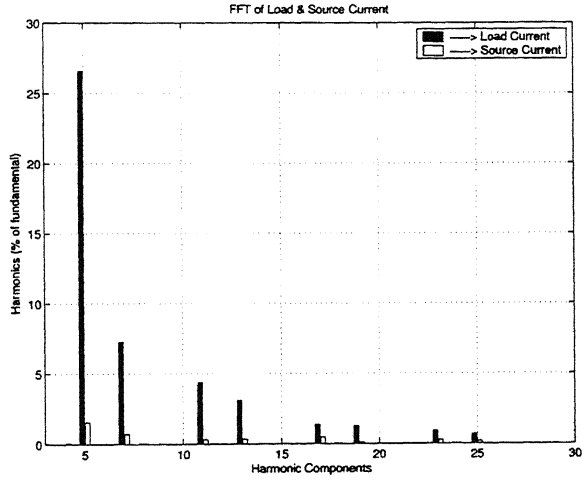

Figure 5.19. FFT of currents for the above case

Fig. 5.18 shows the simulation results at 48Hz supply frequency with mistuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.19. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.75%, 0.85%, 0.35% and 0.35% respectively, which are less than the standard values. It implies, in case of a mistuned passive filter, this much of frequency variation in negative side can take into account by this HPAF.

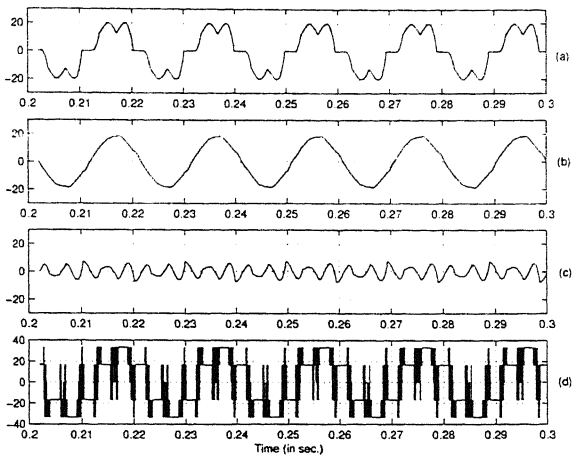

Figure 5.20. Simulation Waveforms at 51 Hz (with mistuned passive filter): (a) Load current (for rectifier type load); (b) Source current; (c) Filter current; (d) Inverter voltage output.

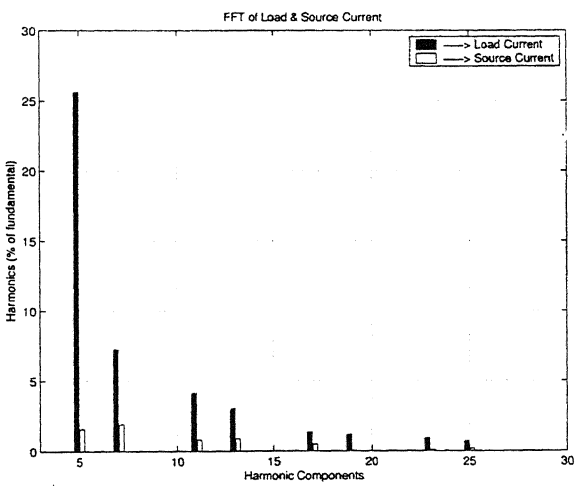

Figure 5.21. FFT of currents for the above case

Fig. 5.20 shows the simulation results at 51Hz supply frequency with mistuned passive filter. The harmonic analysis for the load current and the source current is shown in fig. 5.21. The amount of 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic currents are 1.2%, 2.1%, 0.7% and 0.78% respectively, which are less than the standard values. It implies, in case of a mistuned passive filter, this much of frequency variation in positive side can take into account by this HPAF.

5.3 Discussion

The simulation waveforms at 50 Hz with tuned passive filter is shown in figure5.10. It shows the maximum harmonic parts of load current are supplied by the active filter. After using the hybrid parallel active filter the percentage of harmonic currents in source current becomes within *IEEE standards 519.*

Figure5.2 shows the minimum dc bus voltage for which the source harmonic currents remain within *IEEE standards 519.* The harmonic analysis for this by using *FFT* is shown in figure5.3. In this 5^{th} harmonic current is 4%, 7^{th} harmonnic current is 1.65%, 11^{th} harmonnic current is 2%, 13^{th} harmonnic current is 1.6%, 17^{th} harmonnic current is 1.25% and 19^{th} harmonnic current is 0.5%.

The passive filter is designed in such a way that it blocks the fundamental. But due to leakage resistance of capacitor the impedance offered by the passive filter at fundamental frequency is not infinite. This accounts for the slight mismatch in the fundamental component of the source currents and the load currents. Hence only the harmonic voltage is supplied by the active filter required to source the harmonic currents. As there no need of producing fundamental voltage to cancel out the PCC voltage, this results in a great reduction of the required rating of the active filter. Here the minimum dc-bus voltage is about 25 volts and the current supplied by inverter is around 8 amps, so the required rating of the active filter is 0.2 kVA, which is just 1.6% of 12 kVA load.

Figure5.4 shows the minimum dc bus voltage for which the hybrid parallel active filter works as a harmonic isolator in between load and source, i.e. the total load harmonic currents is supplied by active filter. Negligible harmonic currents remain in source current (figure5.5). For this purpose the inverter rating may goes upto 0.72 kVA, which is 6% of load kVA.

The simulation results for different supply frequencies are shown in figure5.10-5.13. In some power systems, the frequency variation is a common phenomenon. The harmonic currents at different frequency for a tuned passive filter is tabulated in table5.1.

About $\pm 10\%$ variation due to aging and temperature effects on passive filter components have also been taken into consideration. Figure5.18-5.21 shows it does not effect the filter char-

Table 5.1. Results for Tuned Passive Filter

Current Harmonics	48Hz	49Hz	50Hz	51Hz	Maximum Limits
$5^{th}(in\%)$	1.54	1.22	0.84	1.57	4.0
$7^{th}(in\%)$	0.73	1.18	1.67	1.9	4.0
$11^{th}(in\%)$	0.32	0.5	0.5	0.8	2.0
$13^{th}(in\%)$	0.34	0.26	0.55	0.87	2.0
$17^{th}(in\%)$	0.47	0.42	0.64	0.48	1.5
$19^{th}(in\%)$	0.09	0.26	0.3	0.02	1.5
$23^{rd}(in\%)$	0.27	0.28	0.15	0.07	0.6

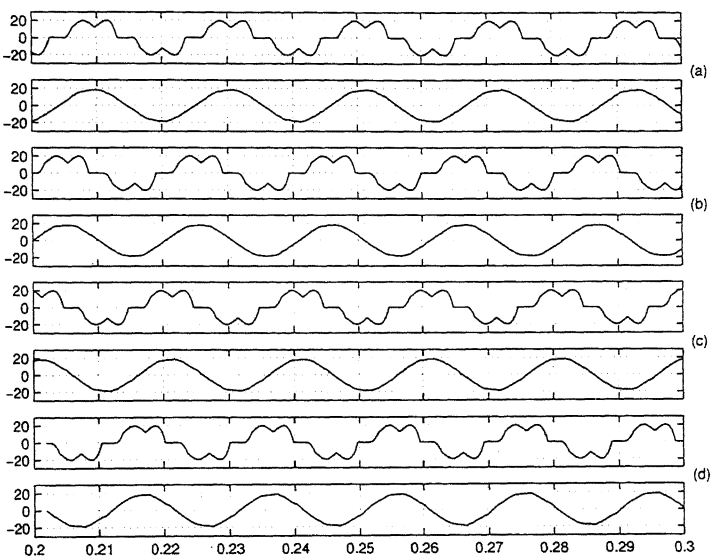

Figure 5.22. Comparison characteristics (with tuned passive filter): (a) Load and source current at 48 Hz; (b) Load and source current at 49 Hz; (c) Load and source current at 50 Hz; (d) Load and source current at 51 Hz.

acteristic significantly. The harmonic currents at differnet frequency for a tuned passive filter is tabulated in table5.2.

From figure5.22 and figure5.23 we can conclude the filtering characteristics are independent of frequency variation within a given range. So in between $48-51$ Hz, the load harmonic currents will be supplied by this hybrid active filter according to the *IEEE standards 519*.

Table 5.2. Results for Mistuned Passive Filter

Current Harmonics	48Hz	49Hz	50Hz	51Hz	Maximum Limits
$5^{th}(in\%)$	1.75	1.5	0.95	1.2	4.0
$7^{th}(in\%)$	0.85	1.25	1.75	2.1	4.0
$11^{th}(in\%)$	0.35	0.5	0.68	0.7	2.0
$13^{th}(in\%)$	0.35	0.27	0.32	0.78	2.0
$17^{th}(in\%)$	0.5	0.35	0.58	0.7	1.5
$19^{th}(in\%)$	0.0	0.25	0.43	0.18	1.5
$23^{rd}(in\%)$	0.25	0.3	0.23	0.09	0.6

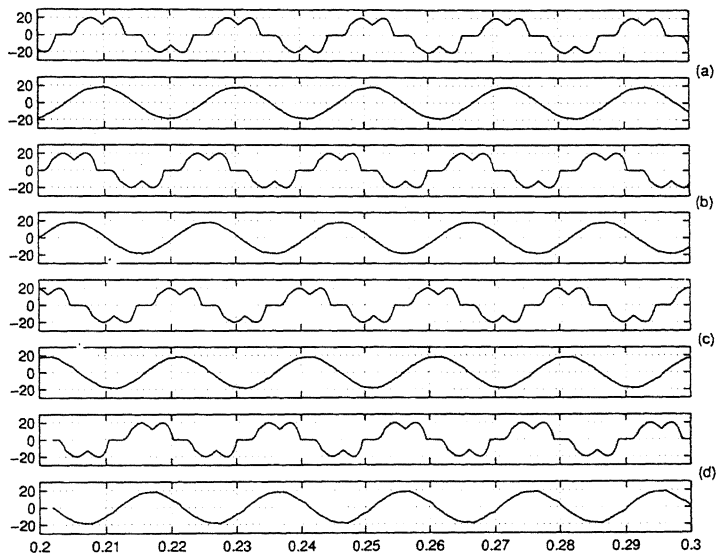

Figure 5.23. Comparison characteristics (with mistuned passive filter): (a) Load and source current at 48 Hz; (b) Load and source current at 49 Hz; (c) Load and source current at 50 Hz; (d) Load and source current at 51 Hz.

5.4 Concluding Remarks

The simulation results show that the proposed hybrid active filter is capable of compensating multiple harmonic components with a small-rating inverter. The required rating of the inverter is 0.2 kVA, which is only 1.6% of load kVA. In the frequency variation range $48 - 51$ Hz it works within *IEEE standards 519*. The passive filter components tolerance have also been taken into consideration and the simulation results show filtering characteristics slightly depend on it.

Chapter 6

Hardware Realization of Sub-modules

The controller part is developed using *TMS320F240 DSP* processor. The different modules are made and tested on it. The module programs for *ADC*, *DAC*, *LED*, input port, output port, *PWM*, phase transformation, low-pass filter, *PI* controller, *PLL* are included in appendix C. A *PLL* is designed and the experimental results are shown, which ensure that the *PLL* is locked not only for balanced supply but also for unbalanced distorted supply.

6.1 Hardware Platform

DigiCon is a *hardware platform* for control software development for *power electronic applications* [29]. DigiCon has *DSP based control hardware* and a power supply module working from the single-phase supply. The digital controller PCB in DigiCon is built around *TMS320F240* Texas DSP. This is a *16 bit fixed point DSP* and it combines the features of enhanced *TMS320* architectural design of the *C2xLP* core for low cost, high performance capabilities and advanced peripherals, which are optimized for power electronic applications. These advanced peripherals include the *Event Manager Module*, which includes 3 general-purpose timers; compare registers, which can generate up to *12 PWM pulses* and a *dual 10-bit ADC*.

Following are the important features available in DigiCon.

- *TMS 320 F240 DSP*

- *12 channels of 12bit, simultaneous sampling ADCs* for reading analog signals.
- *4 channels of DAC* for monitoring different variables during software development.
- *RS 232 Serial Communication interface* for data exchange with other systems.
- *12 PWM Pulses* terminated on FRC connectors with which two independent 3- phase two level converters or one three phase three level converter can be controlled.
- Programmable *Dead-time logic* for complementary PWM pairs
- Status indication with *LEDs*
- *Logic circuitry* to block the gate pulses in the event of faults.
- *3 Digital input channels* with galvanic isolation.
- *8 Digital output channels.*

The controller combines high computing power, enough analog Input channels, PWM Output, digital I/Os, Flash Memory in program space, serial communication interface, DAC outputs for software debugging and system testing etc.

The six-layer layout of the PCB enhances EMI/EMC qualities of the PCB and makes it very compact. This PCB can be used in applications like dual bridge 4-quadrant converters, 3-level Inverters etc. apart from the conventional converters and inverters used in variable speed drives, induction furnace, UPS etc.

For program development and debugging, XDS510PP in-circuit emulator is used.

Two sets of 6 PWMs with programmable dead time are terminated on FRC connectors.

Memory Memory area of the DSP used in this controller is divided into program memory, data memory and I/O memory. The DSP has got internal memory both in program space and data space. Additional external memory is provided on the controller to facilitate easy program development. Different memory blocks of the controller are given below.

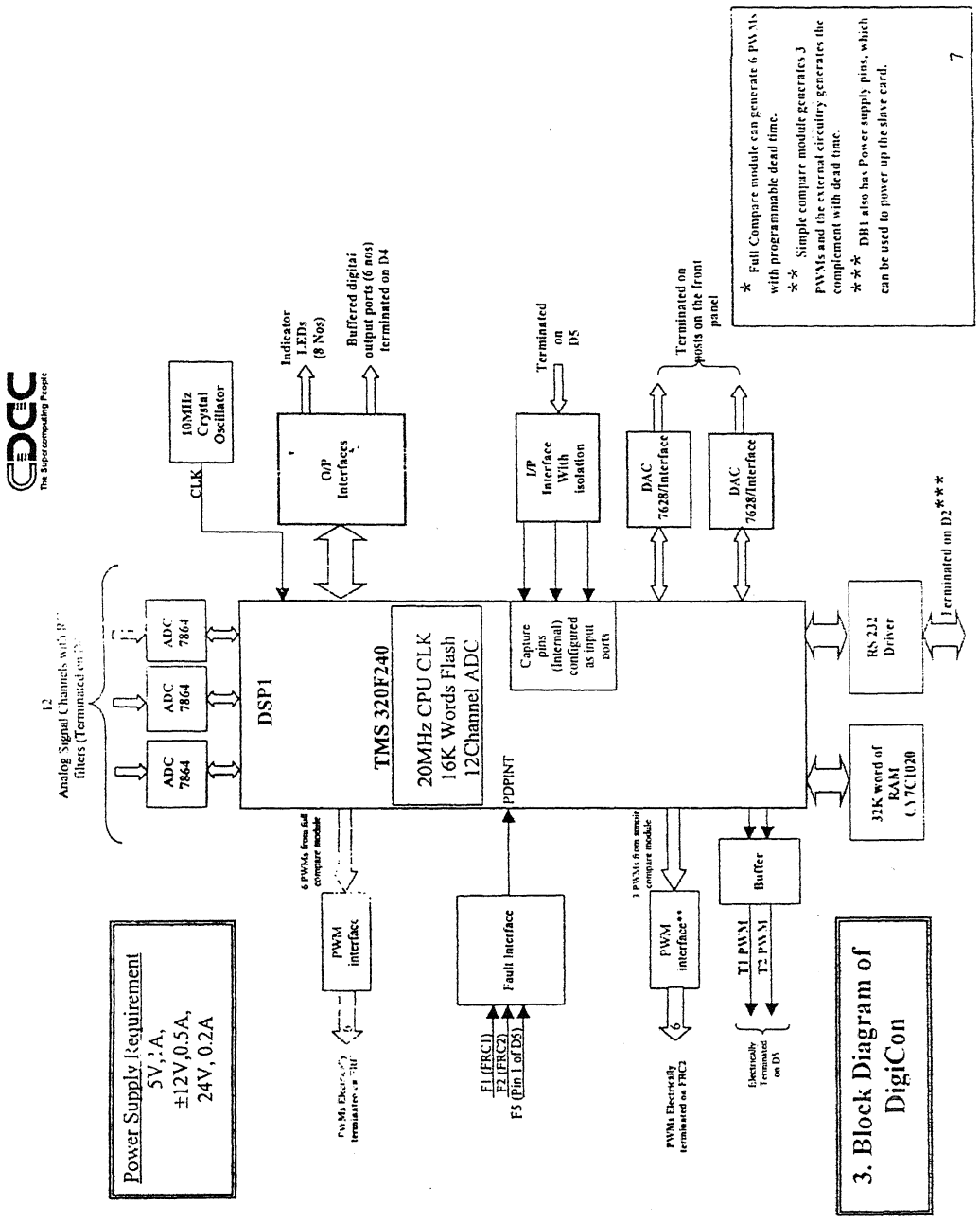

Figure 6.1. Block Diagram of DigiCon

- $16k$ words of internal *EEPROM* (Flash memory) in the program area -ADDRESS: $0000 - 3FFFh$. The software developed can be flashed in this area.
- $32k$ words of external RAM in the program area -ADDRESS: $4000 - BFFFh$. During program development the user may load program to this block of memory. This is to reduce the number of flash writings during development. Once the software is ready it can be flashed.
- 256 words on chip program memory -ADDRESS: $0FE00h - 0FEFFh$. This memory can also be configured as the data memory space of the DSP ADDRESS: $0200h - 02FFh$. Only one mode is possible at a time.
- 288 words of Dual-Access RAM in the data space -ADDRESS: $0060h - 007Fh$ and $0300h - 03FFh$.

Analog to Digital Converter (ADC) To achieve better speed of data acquisition, accuracy and resolution 3 numbers of 4 channel, bipolar, simultaneous sampling, external ADCs (AD 7864) are interfaced with the DSP of the controller PCB. RC filters are provided in all the inputs to the ADC. Each ADC channel has got a maximum conversion time of $1.65\mu s$. But all the three ADCs(Totally 12 Channels) shall be read together. Input range of this ADC is $\pm 10V$.

Digital to Analog Converter (DAC) The board in DigiCon has two, dual channel, 8-bit DACs (AD 7628). The address mapping of different channels is given below.

$DACl$	$DACOUT1$	$0A000h$
	$DACOUT2$	$0A001h$
$DAC2$	$DACOUT3$	$0C000h$
	$DACOUT4$	$0C001h$

PWM Outputs *TMS 320 F240 DSP* is a processor designed specially for power electronics applications. The processor has mainly two sets of programmable PWM ports associated with event manager module comprising of timers, comparators and many control and data

registers, All the PWM outputs of the Event manager of the DSP have been terminated on DigiCon. The digital Controller PCB of DigiCon can generate totally 12 PWMs that are terminated on two FRC connectors FRC1 and FRC2. FRC1 has 6 PWMs generated by the full compare module of the *F240 DSP*.

Input and Output ports Isolated inputs are interfaced with capture input pins of the DSP. These capture pins have to be programmed as input ports in the initialization routine of the code. The input interface allows the user to connect ON/OFF switches for status selection of the system to be controlled. An isolated power supply preferably 24 V may be used in this circuit. This power supply positive shall be connected to Pin 1 of D4. One point of status selection switches shall be connected to Pin 2, Pin6, and Pin7 respectively on D5. The other point of the switches shall be connected to ground of the isolated power supply. The controller has one set of LED (8 nos.) interface with which the user may be used for status display (LED2-LED9 in front panel). 6 buffered output ports (Digital O/P 1-6) are terminated on the D-,Connector D4. User can program T1PWM and T2PWM of the DSP, which are buffered and terminated on the D-connector D5 as output ports.

External Interrupts *TMS 320 F240* has many numbers of external interrupts. The hardware interrupt used in this controller is only the *PDPINT*, which is used for pulse blocking in the event of faults.

Crystal Oscillator The controller uses $10MHz$ crystal oscillator as the clock source. $20MHz$ CPU clock frequency may be generated by appropriately programming the internal PLL Clock module of the DSP. The flash programming utility of Spectrum Digital for $F240$ device takes $10MHz$ by default. So $10MHz$ crystal oscillator is used in this controller. The initialization should program clock control registers convert in input clock frequency of $10MHz$ to $20MHz$.

6.2 Basic Concept of Assembly Language Programming

6.2.1 Scaling

TMS320F240 is a fixed point *DSP*, normally floating point operation is not possible. So scaling is required to handle any type of variable. The following convention is followed to represent floating point variable in a fixed point *DSP*.

$$
\begin{array}{ccc}
07FFFh & ---> & +2 \\
\vdots & & \vdots \\
03FFFh & ---> & +1 \\
\vdots & & \vdots \\
0000h & ---> & 0 \\
\vdots & & \vdots \\
0C000h & ---> & -1 \\
\vdots & & \vdots \\
08000h & ---> & -2
\end{array}
$$

Now any equation can be converted into per unit form and use $03FFFh$ as 1 *perunit*. Some examples are shown in appendix C.

Base value must be chosen in such a way that the maximum value of that variable should not cross 2 *perunit*.

6.2.2 ADC Conversion

Input range of this external *ADC*s (*AD 7864*) is $\pm 10V$. This is a 12-bit *ADC*. So the following table generates 16-bit equivalent word for input range $\pm 10V$.

ADC input	12-bit ADC output	equivalent 16-bit ADC output
$+10V$	$07FFh$	$07FFFh$
$\vdots$	$\vdots$	$\vdots$
$+5V$	$03FFh$	$03FFFh$
$\vdots$	$\vdots$	$\vdots$
$0V$	$0000h$	$0000h$
$\vdots$	$\vdots$	$\vdots$
$-5V$	$0C00h$	$0C000h$
$\vdots$	$\vdots$	$\vdots$
$-10V$	$0800h$	$08000h$

So, (equivalent 16-bit ADC output) = (12-bit ADC output) $\times 2^4$.

6.2.3 DAC Conversion

Output range of this external *DAC*s (AD 7628) is $\pm 10V$. This is a 8-bit DAC. So the following table generates the *DAC* output for any 16-bit word.

16-bit DAC input	equivalent 8-bit DAC input	DAC output
$07FFFh$	$0FFh$	$+10V$
$\vdots$	$\vdots$	$\vdots$
$03FFFh$	$0BFh$	$+5V$
$\vdots$	$\vdots$	$\vdots$
$0000h$	$080h$	$0V$
$\vdots$	$\vdots$	$\vdots$
$0BFFFh$	$03Fh$	$-5V$
$\vdots$	$\vdots$	$\vdots$
$08000h$	$00h$	$-10V$

So, (equivalent 8-bit DAC input) = (16-bit DAC input) / 2^8 + 80h.

6.2.4 Sine Table

A sine table is included in the data memory of 256 words, starting from 0200h. The values of $\sin 0^0$ to $\sin 90^0$ are stored in that data memory space. So the resolution of this sine table is

$$\Delta\theta = \frac{90^0}{256}.$$

So,

0200	$\sin(0)^0$
0201	$\sin(\Delta\theta)^0$
0202	$\sin(2\Delta\theta)^0$
0203	$\sin(3\Delta\theta)^0$
$\vdots$	$\vdots$
$02FFh$	$\sin(90)^0$

Now the value of $\sin(\theta)^0$ can be obtained from the sine table in the following way,

First of all the quadrant is calculated.

Now if the n^{th} location in the data memory (i.e. $0200h + n$) contains the value of $\sin(\theta)^0$ then,

$$n = \frac{\theta}{\Delta\theta}.$$

Next, according to the quadrant, sign of $\sin(\theta)^0$ is chosen.

To get the cos value from the same table we have to add 90^0 with the angle and next the remaining procedure is same as before.

In the similar fashion we can also make the look-up table to get the square-root values.

6.3 PI controller Design in Fixed Point Processor

In frequency domain an integral controller can be represented as

$$\frac{K_I}{s}.$$

Now to transfer it into discrete-time domain *bilinear transformation* is used, i.e.

$$s = \frac{2}{T}\left(\frac{z-1}{z+1}\right).$$

So,

$$\begin{aligned}
\frac{y(s)}{u(s)} &= \frac{K_I}{s} \\
\Rightarrow \frac{y(z)}{u(z)} &= K_I\frac{T}{2}\left(\frac{z+1}{z-1}\right) \\
\Rightarrow (z-1)y(z) &= \frac{K_IT}{2}(z+1)u(z) \\
\Rightarrow y(k+1)-y(k) &= \frac{K_IT}{2}[u(k+1)+u(k)] \\
\Rightarrow y(k+1) &= y(k)+\frac{K_IT}{2}[u(k+1)+u(k)] \\
\Rightarrow y(k) &= y(k-1)+\frac{K_IT}{2}[u(k)+u(k-1)]
\end{aligned}$$

where,

K_I is the integral constant, T is the Sampling time, u is the input and y is the output of the controller.

Now the PI controller in frequency domain is represented by

$$K_P + \frac{K_I}{s}.$$

The discrete equivalent of this is written as follows.

$$y[k] = K_Pu[k] + I[k] + K_I\{u[k]+u[k-1]\} \tag{6.1}$$

where,

$I[k]$ is initial conditions of the integrator, during k^{th} switching interval.

So the equation(6.1) is used in *DSP* platform to build a *PI* controller.

6.4 Low Pass Filter design

The cut-off frequency of the low pass filter is taken as 60 rad/s. So the filter transfer function is represented as

$$\frac{y(s)}{u(s)} = \frac{1}{\frac{s}{60}+1}.$$

The discrete equivalent of this is written as follows.

$$\begin{aligned}
\frac{u(z)}{y(z)} &= \frac{2}{60T}\left(\frac{z-1}{z+1}\right)+1 \\
\Rightarrow 30T(z+1)u(z) &= [(z-1)+30T(z+1)]\,y(z) \\
\Rightarrow 30T(z+1)u(z) &= [(1+30T)z-(1-30T)]\,y(z) \\
\Rightarrow \left(\frac{30T}{1+30T}\right)(1+z^{-1})u(z) &= \left[1-\left(\frac{1-30T}{1+30T}\right)z^{-1}\right]y(z) \\
\Rightarrow \left(\frac{30T}{1+30T}\right)[(u(k)+u(k-1)] &= y(k)-\left(\frac{1-30T}{1+30T}\right)y(k-1)
\end{aligned}$$

$$y(k) = \left(\frac{30T}{1+30T}\right)[(u(k)+u(k-1)] + \left(\frac{1-30T}{1+30T}\right)y(k-1). \tag{6.2}$$

This is implemented in *DSP* as a low pass filter. Sampling time T is taken as $100\mu s$.

6.5 PLL Design and Experimental Results

The phase angle of the utility voltage is a critical piece of information for the operation of most apparatuses as: controlled ac $\leftrightarrow$ dc converters, static *VAR* compensators, cycloconverters, active harmonic filters and other energy storage systems coupled with the electric utility [30]. This information may be used to synchronize the turning on/off of power devices, calculate and control the flow of active/reactive power or transform the feedback variables to a reference frame suitable for control purposes. The angle information is typically extracted using some form of a phase locked loop (*PLL*) [31]. Besides utility interface applications, PLL methods are also used in motor control to estimate the electrical angular speed of the rotor [32, 33]. The quality of the lock directly effects the performance of the control loops in above applications.

Line notching, voltage unbalance, line dips, phase loss, and frequency variations are common conditions faced by equipment interfacing with electric utility. Any PLL used under such conditions should not only be able to phase lock to utility voltages as quickly as possible and maintain lock but also provide low distortion output.

A simple, fast and robust three-phase *PLL* for utility applications with emphasis on operation under distorted utility conditions is used [34]. Ample information is available in literature about *PLL*'s as applied to communication systems. It is our intent to treat the *PLL* system purely as a control problem. The topology used is similar in nature to a field-oriented controller, commonly used for converter/inverter control. A control model of the *PLL* is developed and used for time- and frequency-domain analysis. Recommendations are made for selection of appropriate regulator gains. The *PLL* system is completely implemented in software on a *DSP*.

6.5.1 Principle of Operation

The basic configuration of the *PLL* system is shown in figure 6.2. The phase voltages U_{as}, U_{bs}, U_{cs} are obtained from sampled line to line voltages. These stationary reference frame voltages are then transformed to voltages U_{de}, U_{qe} (in a frame of reference synchronized to the utility frequency) using the 3/2 and e/s transformations. The angle θ^* used in these transformations is

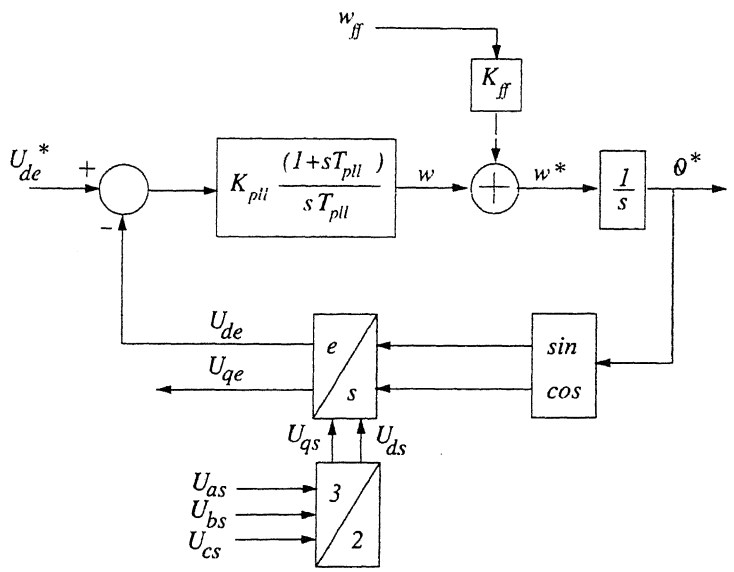

Figure 6.2. Control Diagram of the Phase Locked Loop

obtained by integrating a frequency command ω^*. If the frequency command w* is identical to the utility frequency, the voltages U_{de} and U_{qe} appear as dc values depending on the angle θ^*.

In the given method, a PI regulator is used to obtain that value of θ^* (or ω^*) which drives the feedback voltage U_{de} to a commanded value U_{de}^*. In other words, the regulator results in a rotating frame of reference with respect to which the transformed voltage U_{de} has the desired dc value U_{de}^*. The frequency of rotation of this reference frame is identical to the frequency of the utility voltage. The Magnitude of the controlled quantity U_{de} determines the phase difference between the utility voltages and $\sin(\theta^*)$ or $\cos(\theta^*)$.

The method results not only in the utility frequency ω^* but also allows one to lock at an arbitrary phase angle θ^* with respect to the utility angle θ. The angle $\Delta\theta$ is controlled by the commanded values U_{de}. Analytical development of a simplified model suitable for time/frequency domain analysis follows.

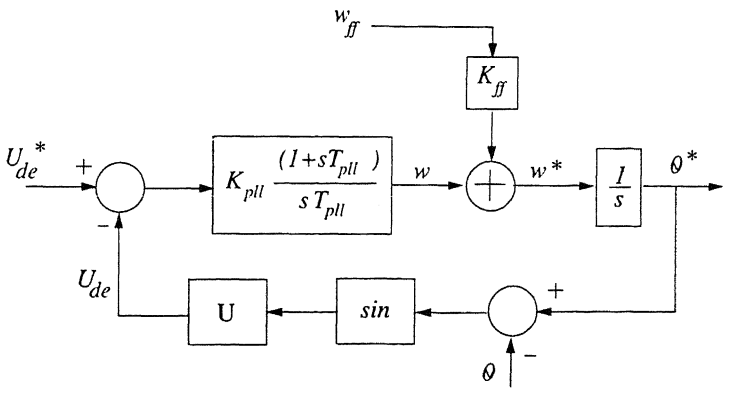

Figure 6.3. Simplified Control Model of the PLL System

6.5.2 Simplified PLL Model

The sampled phase voltages U_{as}, U_{bs}, U_{cs} when transformed to the synchronous frame of reference result in the quadrature voltages U_{de}, U_{qe} (figure 6.2). In vector control scheme, typically two independent regulators are used to control these voltages. In the PLL presented here, only a single control loop is closed around U_{de}. Assuming a balanced three phase utility, a simplified control model of the *PLL* can be developed using the following transformations.

$$\begin{bmatrix} U_{as} \\ U_{bs} \\ U_{cs} \end{bmatrix} = \begin{bmatrix} U\cos(\theta) \\ U\cos(\theta - 2\pi/3) \\ U\cos(\theta - 4\pi/3) \end{bmatrix}, \tag{6.3}$$

$$\begin{bmatrix} U_{qs} \\ U_{ds} \end{bmatrix} = \begin{bmatrix} U_{as} \\ (U_{cs} - U_{bs})/\sqrt{3} \end{bmatrix}, \tag{6.4}$$

$$\begin{bmatrix} U_{qe} \\ U_{de} \end{bmatrix} = \begin{bmatrix} \cos(\theta^*) & -\sin(\theta^*) \\ \sin(\theta^*) & \cos(\theta^*) \end{bmatrix} \begin{bmatrix} U_{qs} \\ U_{ds} \end{bmatrix}. \tag{6.5}$$

Substituting equation(6.3) and (6.4) in equation(6.5), the voltages U_{qe}, U_{de} are given by equation(6.6).

$$\begin{bmatrix} U_{qe} \\ U_{de} \end{bmatrix} = U \begin{bmatrix} \cos(\theta^* - \theta) \\ \sin(\theta^* - \theta) \end{bmatrix} = U \begin{bmatrix} \cos(\Delta\theta) \\ \sin(\Delta\theta) \end{bmatrix}. \tag{6.6}$$

If the error $\Delta\theta$ between the utility angle θ and the *PLL* output θ^* is set to zero, $U_{qe} = U$ and $U_{de} = 0$. This offers immediate possibility to lock onto the utility voltage by regulation of U_{de} to zero. No information is needed about the magnitude U of the utility voltage.

The simplified control model is shown is figure 6.3. For small values of $\Delta\theta$, the term $sin(\Delta\theta)$ behaves linearly, i.e., $sin(\Delta\theta) \sim \Delta\theta$. The *PLL* can thus be treated as a linear control system with the utility magnitude U appearing as a gain in the forward path, the plant being a simple integrator.

With the above configuration, the control problem reduces to picking the correct gains for the model of figure 6.3 for various operating conditions. Taking the sampling delay into account, the plant is a simple lag along with an integrating element (equation(6.7)).

$$H_{plant} = \left(\frac{1}{1+sT_s}\right)\left(\frac{U}{s}\right) \tag{6.7}$$

where,

T_s is the sampling time. The open-loop transfer function H_{ol} with the controller then becomes,

$$H_{ol} = \left(K_{pll}\frac{1+sT_{pll}}{sT_{pll}}\right)\left(\frac{1}{1+sT_s}\right)\left(\frac{U}{s}\right) \tag{6.8}$$

where,

K_{pll}, T_{pll} are the gains associated with the *PI* regulator. This is a standard control problem very similar to a current controlled speed loop of a drive system where the integral term in the plant mimics the mechanical inertia and the lag element emulates the current control loop. Several methods can be used to select the gains based on the desired performance criteria.

The method of symmetrical optimum [35] was used to calculate the regulator gains. According to this method, the regulator gains K_{pll} and T_{pll} are selected such that the amplitude and the phase plot of H_{ol} are symmetrical about the crossover frequency ω_c, which is at the geometric mean of the two corner frequencies of H_{ol}. Given a normalizing factor α, the frequency

$\omega_c, K_{pll}, T_{pll}$ are related as follows.

$$\left.\begin{aligned} \omega_c &= \tfrac{1}{\alpha T_s} \\ T_{pll} &= \alpha^2 T_s \\ K_{pll} &= \tfrac{1}{\alpha U T_s} \end{aligned}\right\}. \tag{6.9}$$

6.5.3 Utility Distortions

When operating on a grid, it is normal to have such utility distortions as: line notching, voltage unbalance, line dip/loss, frequency variation etc. These distortions can pose three possible problems for the *PLL* system.

Polluted PLL Output

Notching of the utility will generate harmonics which will enter the *PLL* loop through the sampled phase voltages U_{as}, U_{bs}, U_{cs} (figure 6.2). While the notches normally will not effect the locking capability of the *PLL*, they will cause harmonics in the *PLL* output, propagating to the associated control utilizing θ^*. Obvious method to eliminate the harmonics is to use filters; either on the sampled voltages or on the error term of the control loop. However, it must be noted that the *PLL* system inherently has strong filtering properties due to the two integrators in series in the forward path. The factor α provides a simple handle to modify the inherent filtering properties of the system without the use of any additional filters.

Loss of Gain

Because the amplitude of the utility voltage appears as a gain term in the forward path (figure 6.3), any dip or unbalance in the line voltage will cause a loss of gain U for the control system. This effect can be eliminated by normalizing the feedback term U_{de} for the utility magnitude U. Calculation of an accurate value of U poses interesting problems if the utility is distorted. As a first approximation: if $U_{de}^* = 0$, the feedback term U_{qe} could be substituted for U. Alternatively, the gains of the PI regulator should be changed to accommodate variations in U.

Phase Deviations

The utility grid is typically a very stiff system as regards to the supply frequency. A deviation in the supply frequency will cause the angle error $\Delta\theta$ to increase. The *PI* regulator naturally works to bring this error to zero. The reaction to frequency fluctuations is thus completely predictable by the closed-loop response of the *PLL* system. The feedforward term ω_{ff} applied through the gain K_{ff} facilitates the function of the regulator to a large extend.

If the supply frequency is inclined to change (e.g., stand alone power systems as diesel generators which are not very stiff), there will be tracking error in the phase angle θ as long as the frequency is changing. If the change in frequency is know, the tracking error can be eliminated by the feedforward term. If the change in frequency is not predictable, an additional integral term may be used in the PI regulator to achieve the same result. This is of use in motor control applications where catching a spinning motor is a common requirement.

6.5.4 Experimental Results

The *PLL* is implemented for a $400V/50Hz$ utility, on a *DSP* with sampling rate of $10kHz$. The *PLL* locks on to the utility voltage quickly and produces a clean output signal (figure6.5).

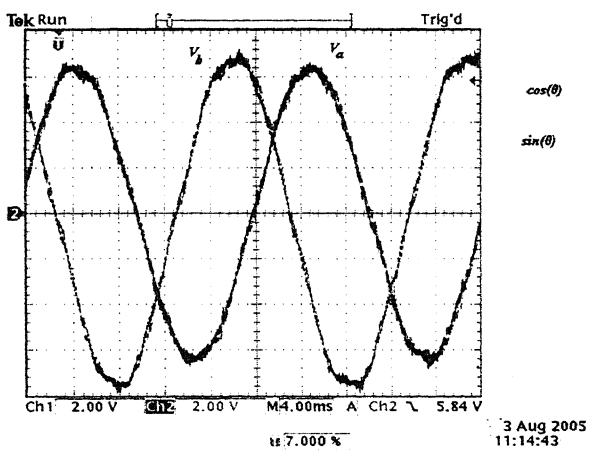

Figure 6.4. Input Voltage V_a and V_b

Figure6.4 shows two phases of the supply voltage. Here the supply is unbalanced.

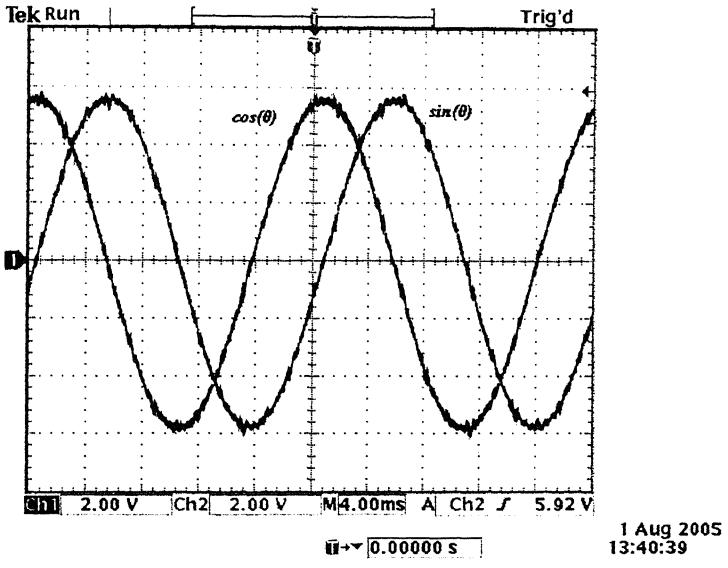

Figure 6.5. *PLL* Outputs

The *PLL* outputs are $\sin(\theta)$ and $\cos(\theta)$ curves, which are shown in figure6.5. It is for the unbalanced supply.

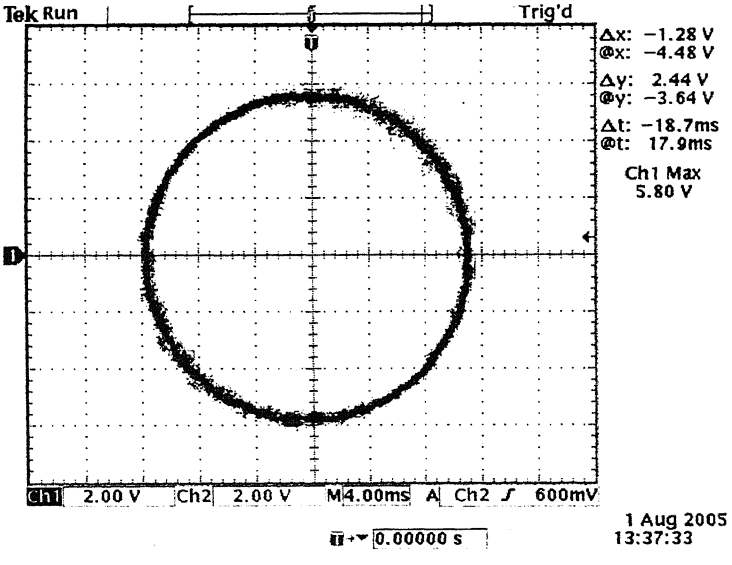

Figure 6.6. Lissajous curve of *PLL* Outputs

Figure6.6 shows the Lissajous curve of the *PLL* outputs for the unbalanced supply.

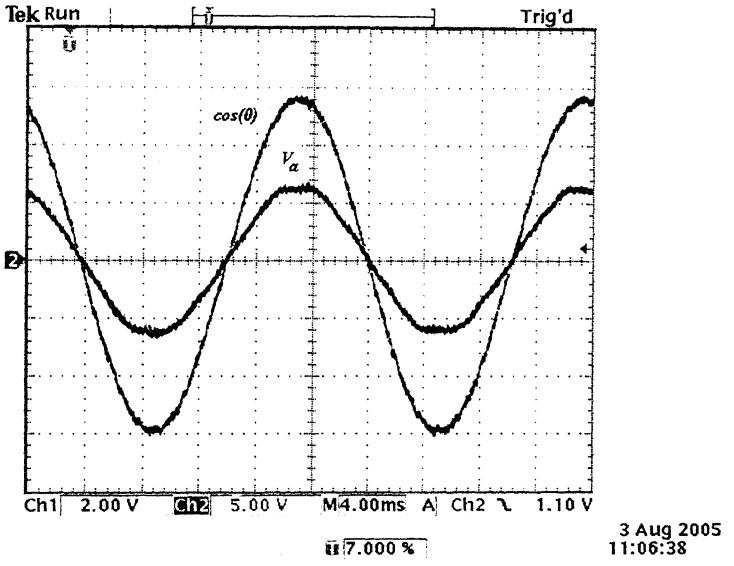

Figure 6.7. Supply Voltage and *PLL* Output

Figure6.7 shows the *PLL* locks on to the unbalanced supply voltage.

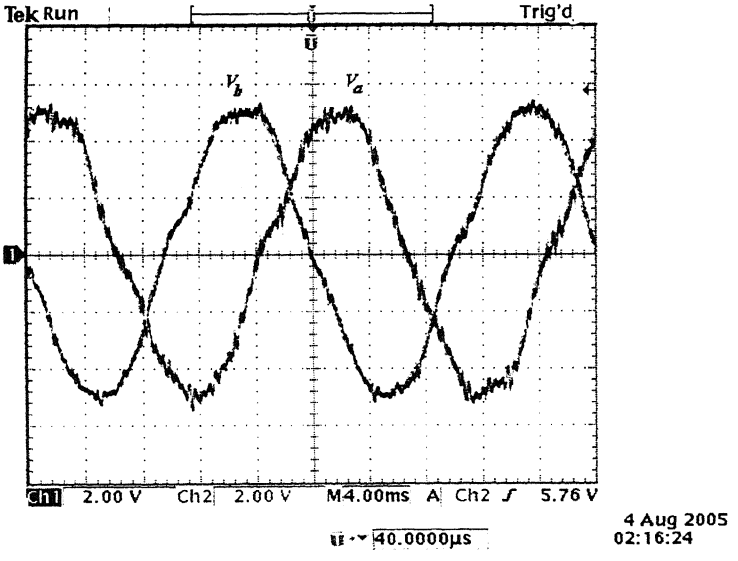

Figure 6.8. Input Voltage V_a and V_b

Two phases of a distorted supply voltage is shown in figure6.8.

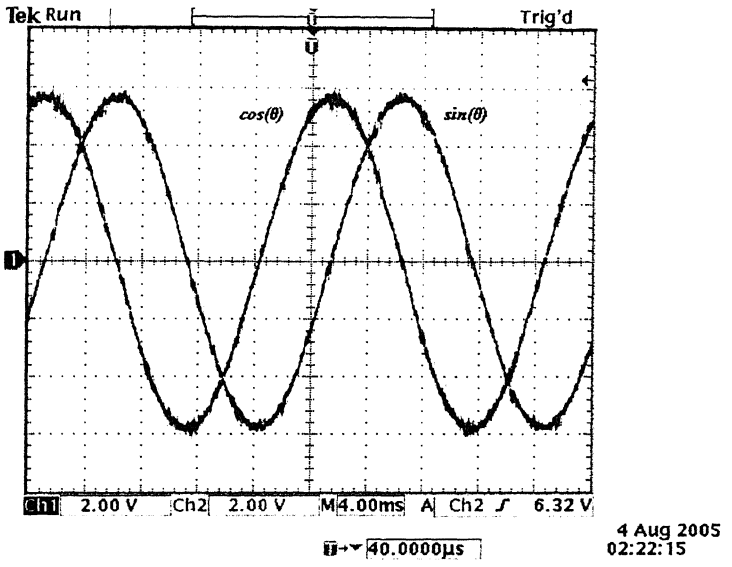

Figure 6.9. *PLL* Outputs

The *PLL* output for a distorted supply is shown in figure6.9.

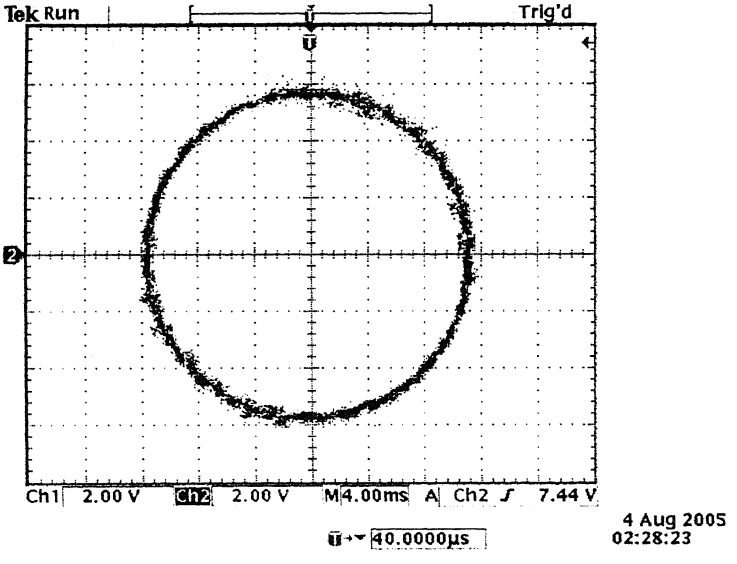

Figure 6.10. Lissajous curve of *PLL* Outputs

Figure6.10 shows the Lissajous curve of the *PLL* outputs for the distorted supply.

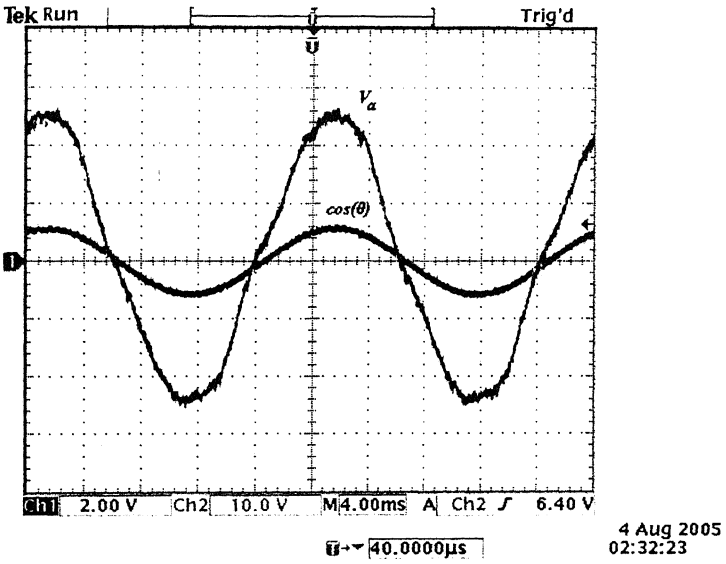

Figure 6.11. Distorted Supply Voltage and *PLL* Output

PLL performance is shown for the case of unbalanced and distorted supply (figure6.11). The *PLL* locks on to the supply voltage.

Discussion

So the *PLL* is working not only with the balanced supply but also with unbalanced distorted supply. It implies that now the angle information can be extracted from the *PCC* by using this *PLL*. The phase angle of the utility voltage is a critical piece of information for the operation of most apparatuses (controlled ac $\leftrightarrow$ dc converters, static *VAR* compensators, cycloconverters, active harmonic filters and other energy storage systems coupled with the electric utility etc.). So now this can be used for $3-2$ or $2-3$ phase transformation in the proposed SRF controller, where the variables of stationary reference frame $(d^s - q^s)$ is transfered to synchronously rotating reference frame$(d^e - q^e)$.

6.6 Concluding Remarks

TMS320F240 DSP processor is used to develop the controller. The main features and architecture of this processor is discussed in detail. *ADC*s are used for reading analog signals and *DAC*s are used for monitoring different variables during software development. Scaling is an important feature in assembly language programming which is discussed with some simple examples. The required conversions for using *ADC* and *DAC* is also shown. The *PI* controller and a low-pass filter is designed in this fixed point processor. The phase transformation module is developed for *SRF* method by using sine table. To follow the phase angle of the utility voltage, *PLL* is designed. This is implemented for a $400V/50Hz$ system. The experimental result shows, the *PLL* locks on to the utility voltage quickly and produces a clean output signal. It is also tested for distorted utility.

Chapter 7

Design and development of Voltage Sensing Card

Electrical voltage sensors measure AC and/or DC voltage levels. They receive voltage inputs and provide outputs as analog voltage signals. Electrical voltage sensors vary in terms of performance specifications, optional features, and environmental operating conditions. Performance specifications include maximum AC voltage frequency, response time, and accuracy. Depending on the device, response times can range from milliseconds to minutes. Accuracy, a percentage amount, represents the difference between a voltage measurement and the actual level.

In this system the supply voltage is $440V$ (line to line rms). The supply voltage signal is used in *ADC* to make the *PLL* module. But the maximum input voltage of the *ADC* is $\pm 10V$. So a voltage sensing card is designed which can generate an equivalent voltage signal of any power circuit voltage, within the range of $\pm 10V$. For this voltage sensing card an isolation amplifier (7800A) is used. It gives the equivalent output voltage signal for a particular input voltage. After that the output is amplified and used in *ADC*.

7.1 Isolation Amplifier

The *HCPL-7800A* high *CMR* isolation amplifier provides a unique combination of features. In a typical implementation the input analog voltage is sensed by the *HCPL-7800A*. A differential output voltage is created on the other side of the *HCPL-7800A* optical isolation barrier. This

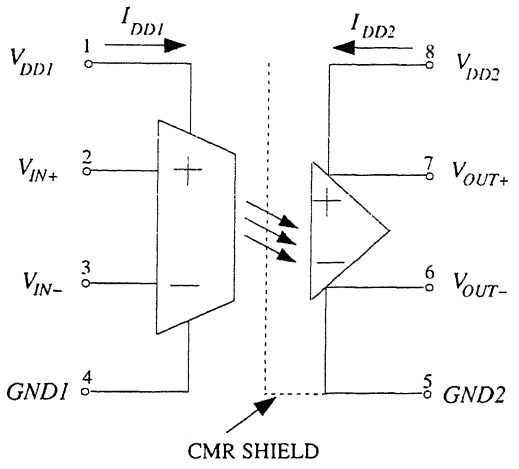

Figure 7.1. Functional Diagram of 7800A

differential output voltage is proportional to the input voltage and can be converted to a single-ended signal by using an op-amp as shown in the voltage sensor circuit diagram.

The *HCPL-7800A* has the following features.

- 15 kV/μ s Common-Mode Rejection at $VCM = 1000V$
- Compact, Auto-Insertable Standard 8-pin *DIP* Package
- 4.6 μV/ ^{0}C Offset Drift vs. Temperature
- 0.9 mV Input Offset Voltage
- 85 kHz Bandwidth
- 0.1% Nonlinearity
- Worldwide Safety Approval: UL 1577 (3750 V rms/1 min), VDE 0884 and CSA
- Advanced Sigma-Delta ($\sigma\Delta$) A/D Converter Technology
- Fully Differential Circuit Topology
- 1 μm *CMOS* IC Technology

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto insertable, industry standard 8-pin *DIP* package that meets worldwide regulatory safety standards (gull-wing surface mount option #300 also available).

The recommended operating conditions are shown in appendix D

In operation, the sigma-delta analog-to-digital converter converts the analog input signal into a high-speed serial bit stream, the time average of which is directly proportional to the input signal. This high speed stream of digital data is encoded and optically transmitted to the detector circuit. The detected signal is decoded and converted into accurate analog voltage levels, which are then filtered to produce the final output signal.

To help maintain device accuracy over time and temperature, internal amplifiers are chopper-stabilized. Additionally, the encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge (both rising and falling) of the converter data to be transmitted, essentially converting the widths of the sigma-delta output pulses into the positions of the encoder output pulses. A significant benefit of this coding scheme is that any non-ideal characteristics of the *LED* (such as non-linearity and drift over time and temperature) have little, if any, effect on the performance of the *HCPL-7800A*.

7.2 Circuit Configuration

The circuit of the voltage sensor is shown in figure7.2. A power supply is regulated to 5 V using a simple three-terminal voltage regulator (7805). The input of the *HCPL-7800A* is connected to the input supply after step it down into ±200mV. The differential output of the isolation amplifier is converted to a ground-referenced single-ended output voltage with a simple differential amplifier circuit. Although the application circuit is relatively simple, a few general recommendations should be followed to ensure optimal performance.

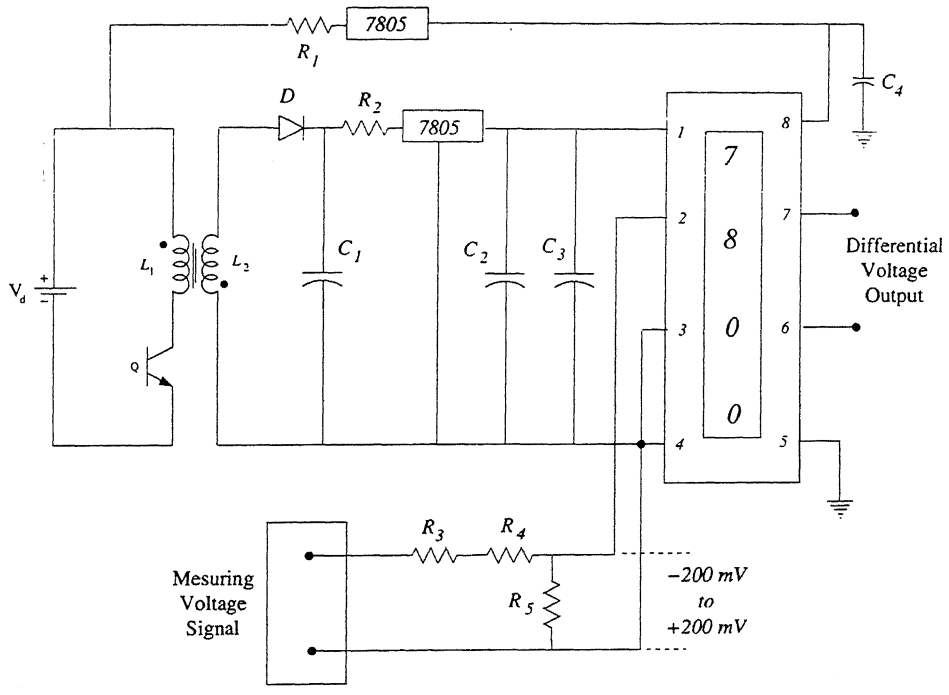

Figure 7.2. Voltage Sensor Circuit

7.3 Design Considerations

As shown in figure7.2, 0.1μF bypass capacitors (C_3 and C_4) should be located as close as possible to the input and output power supply pins of the *HCPL-7800A*. Pin 3 ($VIN-$) is tied directly to pin 4 ($GND1$). A single twisted pair of wire to connect the isolation amplifier to the input voltage. Both input pins are bypassed with 0.1μF capacitors close to the isolation amplifier.

To obtain optimal *CMR* performance, the layout of the printed circuit board (*PCB*) minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground plane on the *PCB* does not pass directly below the *HCPL-7800A*.

A 7805 three terminal voltage regulator is used in the circuit. Because the performance of the isolation amplifier can be affected by changes in the power supply voltages, using regulators with tighter output voltage tolerances will result in better overall circuit performance.

7.4 Signal Amplifier and Filter Design

The op-amp used in the external post-amplifier circuit (shown in figure7.3) should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with *JFET* or *MOSFET* input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate *CMRR* and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

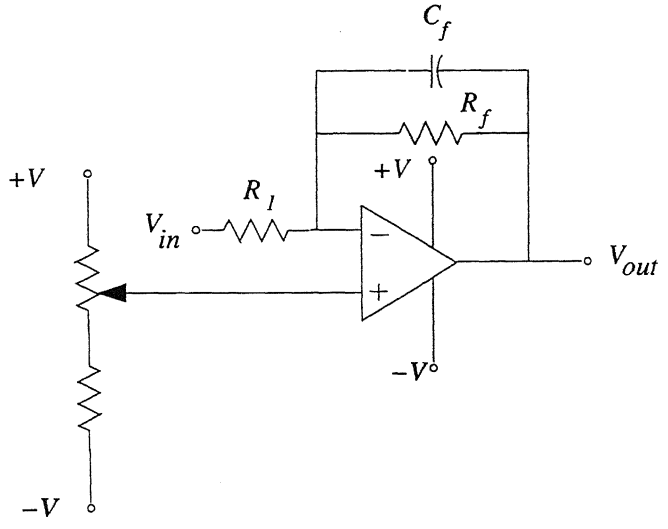

Figure 7.3. Amplifier Circuit

Gain of the amplifier (without C_f) is

$$G = \frac{R_f}{R_1} . \tag{7.1}$$

Gain of amplifier is adjusted to 6.25 to make the final output 10V.

If output of voltage sensor has some noise then this noise will also get amplified by same gain and this will lead to very high noise in output even if original output of voltage sensor has very small amount of noise. So there is need to filter out this noise in pre-amplification stage, this can be done by incorporating a filter in amplifier as shown in figure7.3

Gain of the amplifier

$$G_f = \frac{Z_f(s)}{Z_1(s)} = \frac{G}{1 + R_f C_f s} . \tag{7.2}$$

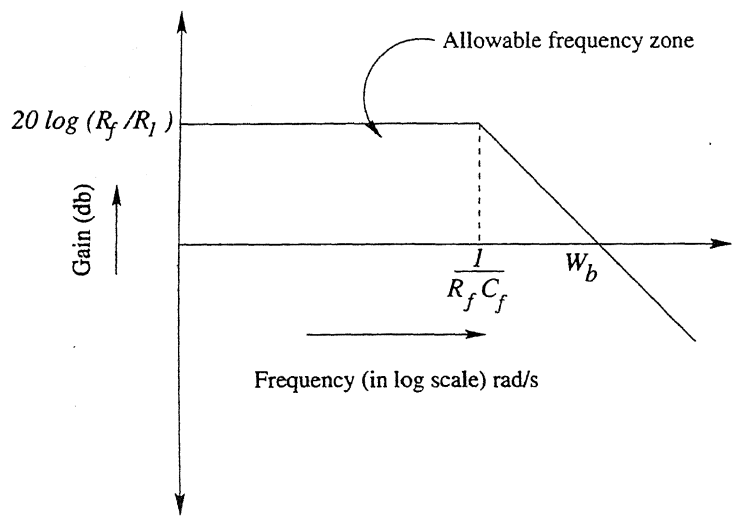

Figure 7.4. Bode Plot of Amplifier with Filter

By selecting proper value of R_f and C_f we can set the corner frequency of RC filter, which will decide the allowable frequency zone. Figure7.4 shows the signals of only certain frequency range will get amplified .

In differential amplifier there is offset voltage because of difference in input bias currents of inverting and non-inverting terminals. Therefore to get the correct output voltage from amplifier

offset voltage is adjusted to small value using potential divider. In potential divider instead of using resistance pot, fixed quarter watt resistances are used. This leads to stable value of resistance in potential divider.

7.5 Fly-back Converter design

An isolated power supply is required for isolation amplifier input side supply. A Fly-back Converter is designed for this purpose [36].

A numerical example of inductor designing for the maximum average current output of 20 mA, is detailed in appendix D.

7.6 PCB Designing

For designing of PCB Protel 99 SE software is used. Prepare a schematic (appendix D) of whole circuit and annotate all the components and specify the footprint of all the component used from component library. If footprint for some component used is not available in the library then make footprint of that component and add this to footprint library, e.g. footprint of isolation amplifier used (7800A) was not available in Protel footprint library. Create a net-list and spreadsheet document of schematic file. Open a pcb file and load the net-list created in previous step, by this way we are transferring all the circuit information of schematic into pcb file (appendix D). Arrange all component as per convenience and after giving design specifications, select option of Auto-routing to get all the connection done automatically by software. Prepare Cam files of this PCB file, This is set of 12 files further used by software Circuit Cam at the time of PCB manufacturing .

Cam-files created in last step are processed in software Circuit Cam and output of this is exported in software Board-master. Board-master software is used to drive the CNC machine used for PCB drilling, milling and rubout. The list of the components used in voltage sensor card is shown in appendix D.

7.7 Observations

The response of the overall isolation amplifier circuit is shown. Figure7.5 shows the input and output waveforms for voltage sensor A. It designed for input voltage 250V (rms) and the output voltage is 9V (rms).

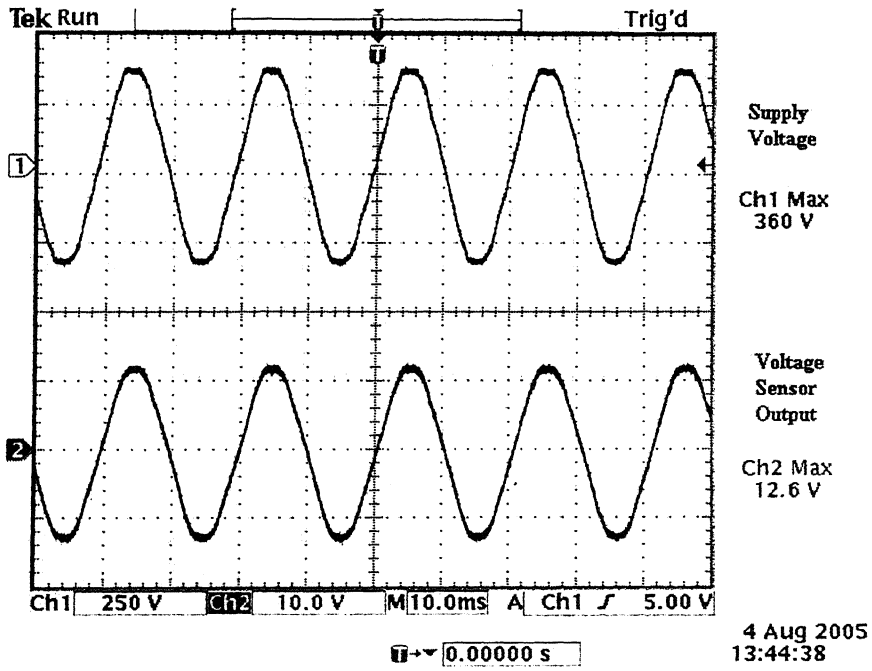

Figure 7.5. Testing Results of Voltage Sensor A

Figure7.5 show the input and output waveforms for voltage sensor B. It designed for input voltage 250V (rms) and the output voltage is 4.5V (rms).

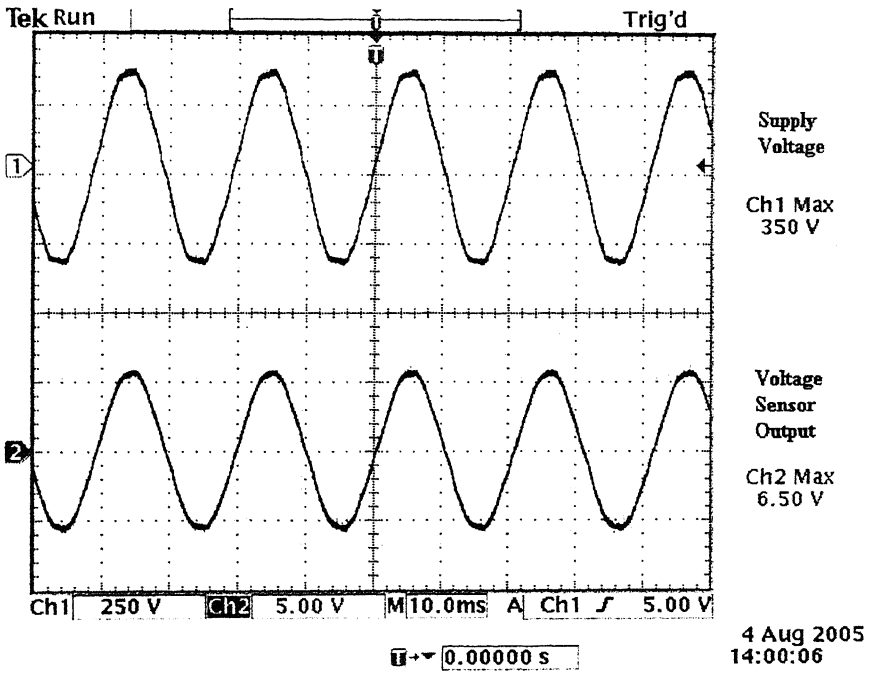

Figure 7.6. Testing Results of Voltage Sensor B

Both figures demonstrate the fast, well-behaved response of the *HCPL-7800A*.

Chapter 8

Conclusions

A novel combined system of a passive and an active filter which are connected in series with each other has been presented with a new control algorithm. Design of control circuit and hardware scheme is discussed in detail. DSP based control platform is developed. A phase lock loop (PLL) system is completely implemented in software on this DSP and tested in a $400V/50Hz$ system. A voltage sensor card is also designed and used in experiment.

The hybrid parallel active filter is chosen in our new model. The new topology is capable of compensating multiple harmonic components depending on its bandwidth. The flow of fundamental current through the hybrid parallel active branch is not allowed, thats why the inverter need not generate any fundamental voltage to cancel out the PCC voltage. It makes the inverter-rating very small. In single tuned hybrid parallel active filter a separate parallel branch is needed to eliminate each harmonic component. But here by using a same rating of inverter we can take care of all the load harmonics. So the cost of total hybrid parallel active filter system becomes very less with respect to the other hybrid active filter systems.

A parallel resonance filter is used in parallel branch of the hybrid active filter in series with the inverter output. The parallel resonance filter is tuned at fundamental ($50Hz$) frequency to block the flow of fundamental through this branch. Since the passive components are not ideal, 10% resistance is concidered for each passive component. The switching harmonics of the high frequency inverter is suppressed by using a switching ripple filter at the inverter output. The

overall passive ciruit characteristic is analised. According to the design consideration the value of the passive circuit components is selected. Since frequency variation in some utility is a common phenomena, so the frequency variation in the range of $48 - 51$ Hz is also taken into consideration. For lower rating of inverter, the dc-bus voltage rating is small.

The dynamic equation of the proposed system is derived. Vector decoupling method is used to simplify the current control law. The control strategy for the new topology is developed. Here synchronous reference frame (SRF) controller is used. Feedback control is implemented. A PI controller is designed to reduce the steady state error. Feedforward control technique is incorporated to achieve better dynamic performance.

The simulation of the new model shows that the proposed hybrid active filter is capable of compensating multiple harmonic components with a small-rating inverter. By using a 0.2 kVA inverter we can supply all the load harmonics for a 12 kVA bridge type rectifier load (highly distorted non linear load). So the hybrid filter rating becomes 1.6% of the load kVA. In the frequency variation range $48 - 51$ Hz it works within IEEE standards 519. The tolerance of the passive filter components have also been taken into consideration. From the simulation result we can conclude, this hybrid parallel active filter works properly with this flexibilities.

The controller is developed by using TMS320F240 DSP processor. The detail of this processor is discussed. The program modules are developed for using ADC, DAC, input, output and PWM channels. The design of PI controller and a low-pass filter in this fixed point processor is also shown. The phase transformation module is developed for SRF method by using sine table. A PLL is designed to follow the phase angle of the utility voltage. This is implemented for a $400V/50Hz$ system. The experimental result shows, the PLL locks on to the utility voltage quickly and produces a clean output signal. It is also works in case of a distorted (with harmonics) supply.

A voltage sensor card is developed. The control circuit input supply is $\pm 15V$. A fly-back inductor is used to generate a isolated $5V$ dc supply for 7800 (isolation amplifier). The output of 7800 is amplified to the desired value. The performance of the developed card is tested. We can use this voltage sensor card to track the PCC voltage. The input range is $350 - 400V$ and the

output range is upto $10V$, which can directly used in ADCs.

The procedure of inductor designing is also laid down. Two inductors are designed, one for power circuit of rating $2mH$ and other one a fly-back inductor used in voltage sensor card. These are made by using ferrite core.

8.1 Scope for Future Work

The theory developed in this thesis was verified analytically and through simulation, which conclusively prove that the proposed approach reduces the inverter rating. It is also independent of supply frequency variation within a certain range. Some parts of the experiment has already been done. So a final experimental verification of the proposed system could probably be carried out.

Appendix A

A.1 Passive Circuit Design

Table A.1. Parallel Resonant Filter Parameters

L_f	103.5 mH, 230 volts, 10 amps
C_f	100 μF, 230 volts, 10 amps, ac capacitor

Table A.2. Circuit Constants

L_i	2 mH, 230 volts, 10 amps
C_{dc}	1000 μF, 100 volts, electrolytic capacitor

Appendix B

B.1 Simulation Parameters

- **Parallel filter components** Circuit parameters are listed below:

	L_f	C_f
tuned	$103.5mH$	$100\mu F$
mistuned	$93.15mH$	$110\mu F$

- **Switching ripple filter components**

$$L_i = 2mH$$

- **Other parameters**

R_{L_f}	0.7Ω
R_{C_f}	0.001Ω
$R_{leakage}$	$500M\Omega$
R_{L_i}	0.06Ω
L_s	$5mH$
R_s	0.16Ω
T_s	$1\mu s$

B.2 IEEE Standards 519-1992

Table B.1. Current Distortion Limits for General Distribution Systems (120V Through 69000V)

Maximum Harmonic Current Distortion in Percent of I_L						
I_{sc}/I_L	Individual Harmonic Order (Odd Harmonics)					TDD
	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even Harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
*All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.						
where I_{sc} = maximum short-circuit current at PCC. I_L = maximum demand load current (fundamental frequency component) at PCC.						

TableB.1 lists the harmonic current limits based on the size of the load with respect to the size of the power system to which the load is connected. The ratio I_{sc}/I_L is the ratio of the short-circuit current available at the point of common coupling (PCC), to the maximum fundamental load current.

Appendix C

C.1 Floating Point Operation on a Fixed Point Processor

Example:6.1. 0.95 can be represented as

$$\begin{aligned} 0.95 &= \frac{0.95 \times 3FFFh}{2^{14}} \\ &= \frac{3CCCh}{2^{14}}. \end{aligned}$$

Example:6.2. 1.37 can be represented as

$$\begin{aligned} 1.37 &= \frac{1.37 \times 3FFFh}{2^{14}} \\ &= \frac{57ADh}{2^{14}}. \end{aligned}$$

C.2 Program Modules

Following are some of the test codes used for validation of different modules of the digital controller.The codes include setting of different control registers for different applications.

Clock Test Program to verify the functioning of different clock modules of *TMS320F240 DSP*.

```
                .mmregs                         ;define symbol names of
                                                ;memory-mapped registers
WDKEY   .set    25h
WDCR    .set    29h
CLKCR0  .set    2ah
CLKCR1  .set    2ch
SYSCR   .set    18h

        .text
        .sect "clock"                           ;program segment starts here.
                                                ;Program is loaded to the internal
                                                ;RAM area of the DSP
        SETC    INTM                            ;global mask for INTM
        SETC    CNF

        LDP     #0h
        SPLK    #0h,IMR                         ;masking all interrupts

        LDPK    #0E0h                           ;page points to 7000h
        SPLK    #06Fh,WDCR                      ;disable watch-dog
        SPLK    #055h,WDKEY                     ;disable watch
        SPLK    #0AAh,WDKEY

        LDPK    #0E0h                           ;page points to 7000h
        SPLK    #0B1h,CLKCR1                    ;CLKIN = 10MHz
                                                ;CPUCLK = CLKIN x 2
        SPLK    #080h,CLKCR0                    ;SYSCLK = CPUCLK/4
        SPLK    #040C0h,SYSCR                   ;CPUCLK on CLKOUT pin
wait:   B       wait
```

ADC Test This program is to test ADC. $-10V$ to $+10V$ may be applied to each channels and the converted digital values can be read from data locations DATA11, DATA12, DATA13 and DATA14.

```
                .mmregs                 ;define symbol names of
                                        ;memory-mapped registers
WDKEY           .set        25h
WDCR            .set        29h
CLKCR0          .set        2ah
CLKCR1          .set        2ch
SYSCR           .set        18h

                .data
tempA           .set        01h
adcChSelect     .set        02h
DATA11          .set        03h         ;Following four variables
DATA12          .set        04h         ;are used as data memory
DATA13          .set        05h         ;location to read ADC data
DATA14          .set        06h

                .text
                .sect "adc"             ;program segment starts here.
                SETC        INTM        ;global mask for INTM
                SETC        CNF         ;DARAM B0 is in program space
                CLRC        OVM

                LDP         #0h
                SPLK        #0h,IMR     ;masking all interrupts

                LDPK        #0E0h       ;page points to 7000h
                SPLK        #06Fh,WDCR  ;disable watch-dog
                SPLK        #055h,WDKEY ;disable watch
                SPLK        #0AAh,WDKEY

                LDPK        #0E0h       ;page points to 7000h
                SPLK        #0B1h,CLKCR1 ;CLKIN = 10MHz
                                        ;CPUCLK = CLKIN x 2
                SPLK        #080h,CLKCR0 ;SYSCLK = CPUCLK/4
                SPLK        #040C0h,SYSCR ;CPUCLK on CLKOUT pin
```

```
                MAR     *,AR3
                LAR     AR3,#0300h
                ZAC
                RPT     #0FFh
                SACL    *+

                LDP     #06h            ;Data variables are from 0300h
readAgain:
                CALL    read_ADC1
                B       readAgain

read_ADC1:                              ;Subroutines for each ADCs(External)
                SPLK    #0Fh,adcChSelect ;Select CH1, CH2, CH3 and CH4.
                OUT     adcChSelect,0000h ;for ADC1 (U7 in PCB)
                NOP
                NOP
                CLRC    xf
                RPT     #0FFh
                NOP
                SETC    xf              ;Start of Conversion is given with
                                        ;XF line
till_EOC1:
                BIOZ    read_Data1
                B       till_EOC1
read_Data1:
                IN      DATA11,0000h
                IN      DATA12,0000h
                IN      DATA13,0000h
                IN      DATA14,0000h

                LACC    DATA11,4
                AND     #0FFFFh
                SACL    DATA11

                LACC    DATA12,4
                AND     #0FFFFh
                SACL    DATA12

                LACC    DATA13,4
                AND     #0FFFFh
                SACL    DATA13

                LACC    DATA14,4
                AND     #0FFFFh
                SACL    DATA14
skip_read:
                RET
```

DAC Test Address of first DAC (U14) is $0A00h$ (OUT A) and $0A001h$ (OUT B)
Address of second DAC (U16) is $0C00h$ (OUT A) and $0C001h$ (OUT B)

```
                .mmregs                 ;define symbol names of
                                        ;memory-mapped registers
WDKEY   .set    25h
WDCR    .set    29h
CLKCR0  .set    2ah
CLKCR1  .set    2ch
SYSCR   .set    18h

                .data
tempA   .set    01h
dacFactor .set  02h
dacData .set    03h

                .text
                .sect "dac"             ;program segment starts here.
                SETC    INTM            ;global mask for INTM
                SETC    CNF             ;DARAM B0 is in program space
                CLRC    OVM
                CLRC    SXM             ;sign extension mode

                LDP     #0h
                SPLK    #0h,IMR         ;masking all interrupts

                LDPK    #0E0h           ;page points to 7000h
                SPLK    #06Fh,WDCR      ;disable watch-dog
                SPLK    #055h,WDKEY     ;disable watch
                SPLK    #0AAh,WDKEY

                LDPK    #0E0h           ;page points to 7000h
                SPLK    #0B1h,CLKCR1    ;CLKIN = 10MHz
                                        ;CPUCLK = CLKIN x 2
                SPLK    #080h,CLKCR0    ;SYSCLK = CPUCLK/4
                SPLK    #040C0h,SYSCR   ;CPUCLK on CLKOUT pin

                LDP     #06h            ;Data variables are from 0300h
                SPLK    #3FF0h,dacFactor ;Scaling Factor for 5V = 3FFFh
```

```
writeAgain:
            CALL    write_DAC1
            RPT     #0FFh
            NOP
            B       writeAgain
write_DAC1:                         ;Subroutines for writing to DAC
            LDP     #06h
            SPLK    #0,tempA
            LT      tempA
            MPY     dacFactor
            PAC
            RPT     #21h
            SFR
            ADD     #80h
            SACL    dacData
            OUT     dacData,0A000h  ;OUT A of DAC1
            RET
```

LED Test This program is to test LEDs. Address of LED port is $06000h$.

```
            .mmregs             ;define symbol names of
                                ;memory-mapped registers
WDKEY       .set    25h
WDCR        .set    29h
CLKCR0      .set    2ah
CLKCR1      .set    2ch
SYSCR       .set    18h

            .data
tempA       .set    01h

            .text
            .sect "led"         ;program segment starts here.
            SETC    INTM        ;global mask for INTM
            SETC    CNF         ;DARAM B0 is in program space
            CLRC    OVM
            CLRC    SXM         ;sign extension mode

            LDP     #0h
            SPLK    #0h,IMR     ;masking all interrupts
```

```
                LDPK    #0E0h           ;page points to 7000h
                SPLK    #06Fh,WDCR      ;disable watch-dog
                SPLK    #055h,WDKEY     ;disable watch
                SPLK    #0AAh,WDKEY

                LDPK    #0E0h           ;page points to 7000h
                SPLK    #0B1h,CLKCR1    ;CLKIN = 10MHz
                                        ;CPUCLK = CLKIN x 2
                SPLK    #080h,CLKCR0    ;SYSCLK = CPUCLK/4
                SPLK    #040C0h,SYSCR   ;CPUCLK on CLKOUT pin

                LDP     #06h            ;Data variables are from 0300h
                SPLK    #08h,tempA      ;LED5 is OFF and all others are ON
writeAgain:
                CALL    write_LEDport
                B       writeAgain
write_LEDport:                          ;Subroutines for writing to LED
                OUT     tempA,06000h
                RET
```

OUTPUTPORT Test This program is to test output ports. Address of output port is $08000h$.

```
                .mmregs                 ;define symbol names of
                                        ;memory-mapped registers
WDKEY   .set            25h
WDCR    .set            29h
CLKCR0  .set            2ah
CLKCR1  .set            2ch
SYSCR   .set            18h

                .data
tempA   .set            01h

                .text
                .sect "outputports"     ;program segment starts here.
                SETC    INTM    ;global mask for INTM
                SETC    CNF     ;DARAM B0 is in program space
                CLRC    OVM
                CLRC    SXM     ;sign extension mode
```

```
                LDP     #0h
                SPLK    #0h,IMR         ;masking all interrupts

                LDPK    #0E0h           ;page points to 7000h
                SPLK    #06Fh,WDCR      ;disable watch-dog
                SPLK    #055h,WDKEY     ;disable watch
                SPLK    #0AAh,WDKEY

                LDPK    #0E0h           ;page points to 7000h
                SPLK    #0B1h,CLKCR1    ;CLKIN = 10MHz
                                        ;CPUCLK = CLKIN x 2
                SPLK    #080h,CLKCR0    ;SYSCLK = CPUCLK/4
                SPLK    #040C0h,SYSCR   ;CPUCLK on CLKOUT pin

                LDP     #06h            ;Data variables are from 0300h
                SPLK    #00h,tempA      ;LED5 is OFF and all others are ON
writeAgain:
                CALL    write_outport
                B       writeAgain
write_outport:                          ;Subroutines for writing to outport
                OUT     tempA,08000h    ;Port with
                                        ;d0 - Bit for blocking PWM
                                        ;d1 - Bit for resetting faults
                                        ;OPIN1-OPIN - Digital output ports
                RET
```

INPUTPORT Test This program is to test inpút ports of DSP.

```
                .mmregs         ;define symbol names of
                                ;memory-mapped registers
WDKEY           .set    25h
WDCR            .set    29h
CLKCR0          .set    2ah
CLKCR1          .set    2ch
SYSCR           .set    18h
OCRB            .set    12h
PCDATDIR        .set    1ch
```

```
        .data
tempA   .set            01h

        .text
        .sect "inputports"          ;program segment starts here.
        SETC            INTM        ;global mask for INTM
        SETC            CNF         ;DARAM B0 is in program space
        CLRC            OVM
        CLRC            SXM         ;sign extension mode

        LDP             #0h
        SPLK            #0h,IMR     ;masking all interrupts

        LDPK            #0E0h       ;page points to 7000h
        SPLK            #06Fh,WDCR  ;disable watch-dog
        SPLK            #055h,WDKEY ;disable watch
        SPLK            #0AAh,WDKEY

        LDPK            #0E0h       ;page points to 7000h
        SPLK            #0B1h,CLKCR1 ;CLKIN = 10MHz
                                    ;CPUCLK = CLKIN x 2
        SPLK            #080h,CLKCR0 ;SYSCLK = CPUCLK/4
        SPLK            #040C0h,SYSCR ;CPUCLK on CLKOUT pin

        LDP             #0E1h
        SPLK            #00h,OCRB   ;Configure I/O control registers
        SPLK            #00h,PCDATDIR ; for input ports.
start:
        LDP             #0E1h
        LACC            PCDATDIR
        AND             #040h
        BCND            auto,NEQ
        LDP             #06h
        SPLK            #0FCh,tempA
        CALL            write_LEDport
auto:
        LDP             #0E1h
        LACC            PCDATDIR
        AND             #040h
        BCND            contfb,NEQ
        LDP             #06h
        SPLK            #0F3h,tempA
        CALL            write_LEDport
```

```
contfb:
                LDP     #0E1h
                LACC    PCDATDIR
                AND     #020h
                BCND    start,NEQ
                LDP     #06h
                SPLK    #0CFh,tempA
                CALL    write_LEDport
                B       start
write_LEDport:                          ;Subroutines for writing to LEDport
                OUT     tempA,06000h
                RET
```

Appendix D

D.1 Isolation Amplifier 7800A

Table D.1. Recommended Operating Conditions

Parameters	Min.	Max.
Ambient Operating Temperature (T_A) in ^{0}C	-40	85
Supply Voltage (V_{DD1}, V_{DD2}) in V	4.5	5.5
Input Voltage (accurate and linear) (V_{IN+}, V_{IN-}) in mV	-200	200
Input Voltage (functional) (V_{IN+}, V_{IN-}) in V	-2	2

D.2 Components used in Voltage Sensor Card

Components	Footprint	Quantity	Designator
NE555P	DIP8	1	NE555
Transistor	TO-39	1	Q
Inductor	INDUCT-1605	1	IND
7805	SIP-3	2	VS1,VS2
7800A	DIP8	1	7800A
OpAmp	DIP14	1	Op-Amp
Diode	DIODE-0.4	2	D1, D,2
Capacitor	CAPACITOR	6	C1, C2, C3, C4, C5, C6
Resistor	AXIAL-0.3	20	R1, R2 R3, R4 R5, R6 R7, R8, R9, R10, R11 R12, R13, R14, R15, R16, R17, R18 R19, R20

Table D.2. Components used in Voltage Sensor Card

D.3 Inductor Designing

1. Let the turn ratio be "1", then for V_i=15 V and V_0=6 V

$$\begin{aligned} V_o/V_i &= N_2/N_1 * (D/(1-D)) \\ D &= 0.2857 \end{aligned} \tag{D.1}$$

2. The peak value of current through L_1,

$$\begin{aligned} I_{1peak} &= N_2/N_1 * I_{2peak} = N_2/N_1 * (2 * I_{2avg}) * 1/(1-D) \\ I_{1peak} &= 56mAmp \end{aligned} \tag{D.2}$$

The rms vale of current I_1,

$$\begin{aligned} I_{rms} &= I_{1peak} * \sqrt{D/3} \\ I_{rms} &= 32.3mAmp \end{aligned} \tag{D.3}$$

3. So the inductance L_1 is,

$$\begin{aligned} L_1 &= V_i * D * T/I_{1peak} \\ L_1 &= 25.5mH \end{aligned} \tag{D.4}$$

4. The area product,

$$\begin{aligned} A_i * A_w &= L_1 * I_{1peak} * I_{rms}/B_m * k_w \\ A_i * A_w &= 209mm^4 \end{aligned} \tag{D.5}$$

5. Selecting area product from core table which smallest and higher than obtained in last step

[37, 38]

$$A_i * A_w = 763mm^4 \tag{D.6}$$

Corresponding core and window areas area $A_i = 19.4mm^2$ and $A_w = 39.33mm^2$. core type is EE-1605[37]

6. Calculating number of turns for L1,

$$\begin{aligned} N_1 &= (L_1 * I_{1peak})/(A_i * B_m) \\ N1 &= 217 \end{aligned} \tag{D.7}$$

(taking the nearest integer)

7. The cross section of a single conductor,

$$\begin{aligned} a_{cu} &= I_{rms}/J \\ a_{cu} &= 0.01mm^2 \end{aligned} \tag{D.8}$$

8. Selecting cross section from wire table which is smallest and higher than calculated in last step 0.0158 mm^2 Outer diameter=0.142 mm Nominal diameter = 0.122 mm

9. The air gap length,

$$\begin{aligned} l &= A_i/(\frac{(A_i * B_m)}{(\mu_0 * N * I_{1peak})} - \frac{(a+d)}{N_g}) \\ l &= 0.0225mm \end{aligned} \tag{D.9}$$

Total number of air gaps are two,so there will be two air gaps of 0.0112 mm each

10. The peak flux density,

$$\begin{aligned} B_m &= (L_1 * I_{1peak})/(A_i * N_1) \\ B_m &= 0.3393T \end{aligned} \tag{D.10}$$

which is less than nominal value of this core material.

11. Total conductor area for $L1$,

$$AT_1 = N_1 * A_{cu} * = 3.44mm^2 \tag{D.11}$$

where,

$$A_{cu} = (\pi/4) * (outerdia)^2$$

12. Since turns ratio is unity hence $N_2 = 217$.

So the inductance L_2 is,

$$\begin{aligned} L_2 &= (N_2 * L_1 * I_{1peak})/(N_1 * I_{2peak}) \\ L_2 &= L_1 = 25.5mH \end{aligned} \tag{D.12}$$

13. Sum of total conductor area $A_T = 2 * A_{T1}/k_w = 34.38mm^2$

$$A_w/A_T = 1.144 \tag{D.13}$$

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